AN ABSTRACT OF THE DISSERTATION OF

Spencer Leuenberger for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on December 7, 2017.

Title: Ring Amplifier Design Techniques for High-Precision and High-Speed Amplification

Abstract approved: _____

Un-Ku Moon

Demands of today's integrated society dependent on communication systems have driven the creation of ever more efficient analog-to-digital converters. For the same reasons, digital circuitry has rapidly expanded to serve all the different systems and needs of consumers. The trend of technology development has been to make these digital circuits more efficient. This has led to a degradation of key analog parameters which make the ubiquitous operation amplifier less efficient. Ring amplifiers are an emerging circuit meant to replace the operational amplifier. This dissertation details the design and operation of ring amplifiers. It presents two prototype analog-to-digital converters using ring amplifiers. One ring amplifier employs the use of current-starved inverters and a dynamic deadzone to achieve 74 dB signal-to-noise-distortion ratio at 20 MSPS in a 180 nm complementary metaloxidesemiconductor process. Another ring amplifier using a correlated level

shifting scheme to achieve 74 dB signal-to-noise-distortion ratio at 40 MSPS is presented.

Ring Amplifier Design Techniques for High-Precision and High-Speed Amplification

by

Spencer Leuenberger

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented December 7, 2017
Commencement June 2018

Doctor of Philosophy dissertation of Spencer Leuenberger presented on December 7, 2017.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Spencer Leuenberger, Author

ACKNOWLEDGEMENTS

First, I would like to thank my advisor Dr. Moon. Without you none of this would have happened. When you asked me if I wanted to join your research group I had only a small idea of what it would entail. You've allowed me to grow and seek academic heights I would have not have envisioned before I joined. As a research advisor, you are the best. You allowed me to develop my own ideas but are always willing to give suggestions and feedback. Thank you from the bottom of my heart.

To my committee members Dr. Temes, Dr. Mayaram, and Dr. Natarajan, thank you for providing advice over my five years here in graduate school. Without great professors like you, this university could not provide students here with outstanding opportunities for success.

To my former friends and researchers of Dr. Moon's group Hari, Mani, Taewhan, Allen, Simon, Jason, Yang, Farshad, Brandi, Jerry, and Tim, thanks for all the support and great times. To the current and future students such as Praveen, Calvin, Ahmed, Bohui and Michael, I wish you the best going forward. I hope my occasional crankiness hasn't disrupted you too much. My best advice to you going forward is to get lots of sleep!

To my Mom and Dad, you have been an unyielding pillar of support, giving me the motivation to keep going when I waivered. Thanks for always being there and making this time one without too much strife. To my friends, thanks for always providing me with laughs. It's more important than one may think.

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Chapter 1: Introduction

This dissertation is concentrated on the topic of ring amplifiers. Ring amplifiers are implemented complementary metal oxide semiconductor (CMOS) processes. They are used in the implementation of analog-to-digital converters (ADC). They can be used to efficiently and accurately amplify signals in switched-capacitor circuits. The goal of circuit design is to reduce the power and area of an ADC without a loss in performance. ADC's are a ubiquitous circuit in today's world. As their name suggests they translate analog signals into a digital representation. Once a signal has been converted to the digital domain, signal processing occurs there.

Digital signal processing offers advantages over analog signal processing. It allows for noise immunity as digital signals are saved as one of two levels, a 1 or a 0. One modern use of ADCs is the smartphones seen in Figure 1.1. The radio in a smartphone will process many different signals which include but are not limited to voice communication and internet protocol packets. This information is propagated by base stations across the electromagnetic spectrum. It is received at the antenna and radio frequency circuitry at the front-end of receiver. At the backend is an ADC which digitizes the input.

The march of technology has produced ever smaller circuits that consume less power. Added functionality can be added to phones such as microprocessors when this occurs to the radio eventually leading to the development of software appli-

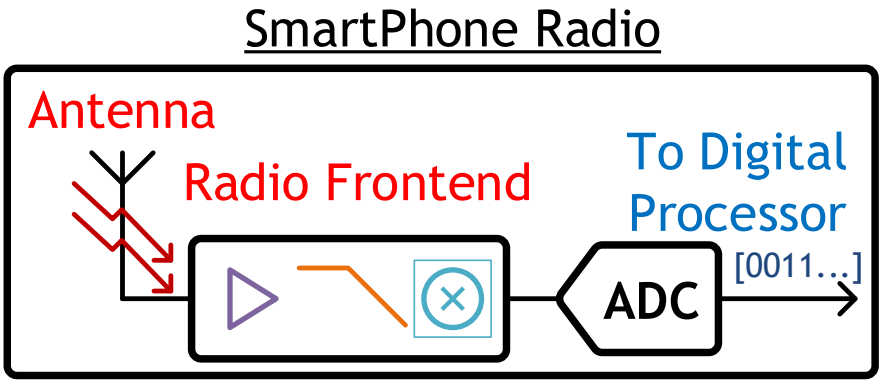


Figure 1.1: A representation of a smartphone radio with an analog-to-digital converter is presented.

cations as added features for phones. The microprocessor still critically relies on ADCs and conversely digital-to-analog converters (DAC) to interact with the outside world. Data converters are a critical part of any modern digital system that interacts with the real (analog) world.

1.1 Motivation

The primary motivation that spurred the development of the techniques described in this dissertation is process scaling in deep sub-micron processes. Technology development has been optimized for digital systems. However, the desire still remains to integrate ADCs and other analog circuitry into the same chip as digital circuitry. This lowers the overall size of the system and is cheaper to implement. Unlike digital circuits that perform well with process scaling the same is not true for analog circuits. Devices have become faster, but parameters related to gain and output swing have degraded. Matching of devices, often critical to ADCs, has

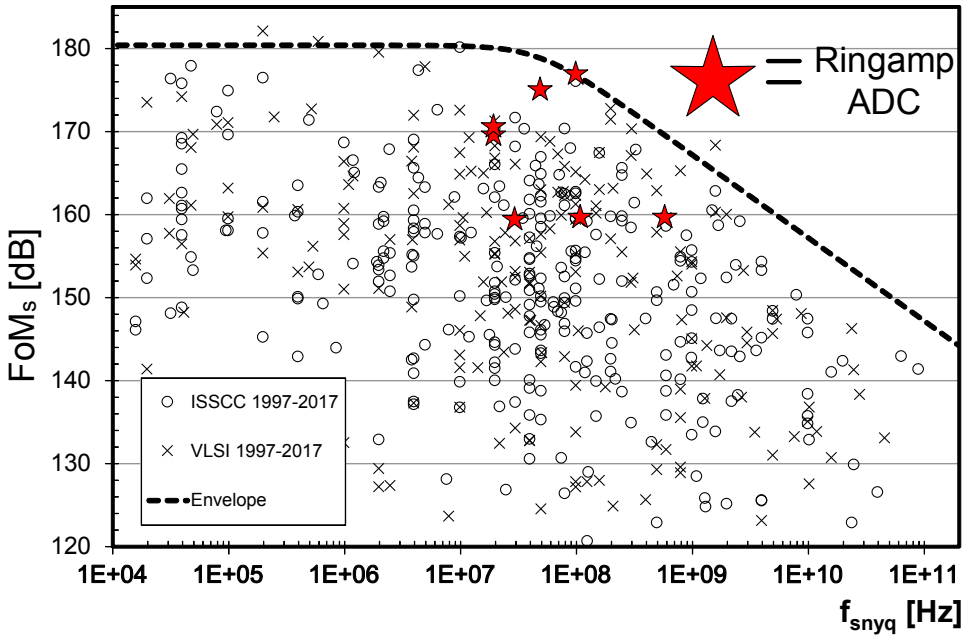


Figure 1.2: A plot of ADC performance versus Nyquist input frequency with ring amplifier based ADCs highlighted.

not improved either.

If an ADC design were ported directly from one process technology to the next, the performance and efficiency may improve or it may not. In addition, there is no guarantee that the ADC will occupy less area due to matching concerns. For an analog circuit designer, these problems mean new solutions need to be developed for modern CMOS processes. One of those new novel techniques is the ring amplifier, which is the topic of this dissertation.

Ring amplifiers have been used as very efficient replacements of operational amplifiers (OpAmp) used as residue amplifiers in pipelined ADCs. The properties of ring amplifiers allow for reduced circuit requirements compared to OpAmps.

The impact of ring amplifiers is seen in Figure 1.2. It is a survey of ADCs from top solid-state circuits conferences [1]. The y-axis is a figure-of-merit for ADC performance (FoM), and the x-axis is Nyquist input frequency. The upper-right of the graph corresponds with state-of-the-art designs. Ring amplifier based ADC's are highlighted. They show excellent performance in the range of 10 MHz to 1 GHz.

1.2 Contribution

The main contributions highlighted in this dissertation are related to ring amplifier circuits. One is the development of a new ring amplifier structure that uses current-starved inverters. The current-starved inverter structure allows for the use of dynamic biasing that can be used to increase performance of ring amplifiers. A prototype pipelined ADC incorporating the current-starved inverter ring amplifiers was fabricated and measured in a 180 nm CMOS process. This ADC achieved 74 dB SNDR with a sampling frequency of 20 MHz while consuming 2.74 mW.

Another important aspect of ring amplifiers explored by the first prototype was their noise performance. The ADC was designed to be amplifier noise limited. This allowed comparisons between transient noise simulations and real life measurements.

The current-starved inverter ring amplifier was further explored in another pipelined ADC. The observation is made that low gain ring amplifiers posses the best settling performance. A dual-path ring amplifier was then designed to take

advantage of this property. Incorporated with a switched-capacitor circuit technique to increase the gain of an amplifier, the prototype ADC is able to achieve 72.5 dB SNDR at 40 MHz operation. Designed in a 180 nm CMOS process, it achieves the fastest operation of a ring amplifier in that process node.

1.3 Organization

This dissertation is organized as follows. Pipelined ADCs are covered in Chapter 2. This chapter is not meant to be a comprehensive review of Pipelined ADC. The main purpose is to build a justification for high open-loop residue amplifiers. Techniques separate from the ring amplifier developed for pipelined ADCs in deep sub-micron processes are reviewed. Ring amplifier operation in switched-capacitor circuits is explained in Chapter 3. In particular, bandwidth of ring amplifiers is explored, and OpAmps are used as comparison point. The result shows that ring amplifiers do not posses the same tradeoffs and trends as OpAmps. This result suggests that ADC system level design can be expanded by the use of ring amplifiers.

The two prototype ADCs are documented in the following chapters. In Chapter 4 the current-starved inverter is introduced. The principles of a dynamic deadzone are explored. An important topic in this chapter is the noise performance of ring amplifiers. The design and measurements of the prototype 15b ADC in 180 nm CMOS that incorporated these topics is covered. Chapter 5 introduces the fact that ring amplifier settling performance is greatly determined by transis-

tor devices sizes. Attempts to increase gain in ring amplifiers through traditional methods result in poor performance. Instead a dual-path ring amplifier for use in a correlated-level shifting scheme is explained. This allows for the fastest settling ring amplifiers in a particular technology to also achieve high gain. This design was demonstrated in a 17b pipelined ADC in 180 nm CMOS.

Chapter 2: Pipelined ADC Design and Prior Work

2.1 Introduction

This dissertation is concentrated on the topic of ring amplifiers. The work presented in this thesis uses ring amplifiers as a residue amplifier in pipelined ADCs. Residue amplifiers are used in ADCs to amplify the difference between an input-signal and recreated estimate of that input from a ADC_{sub}. Traditionally operational amplifiers (OpAmps) are used for this purpose. Ring amplifiers do not possess the same design tradeoffs as an OpAmp. Ring amplifiers can be designed for greater efficiency than an OpAmp.

To appreciate the properties of ring amplifiers in comparison to an OpAmp, it is necessary to first understand the existing constraints and designs. ADC architectures will be briefly summarized leading to the pipelined ADC. Pipelined ADCs inherently use residue amplification techniques. These techniques will be briefly covered with the constraint of using only a single-pole OpAmp. This analysis is used to gain insight into design problems encountered by OpAmps in deep submicron CMOS processes. Recent prior work that has presented novel solutions to the scaling problem in pipelined ADC will be reviewed. This will lead to introduction of a ring amplifier as a replacement for OpAmps in switched-capacitor circuits.

2.2 Analog-to-Digital Converters

Analog-to-digital converters (ADC) perform the action of quantization on their input signals. Quantization is the process of constraining large sets of data, often continuous, to a smaller discrete set. Any real world signal possesses effectively an infinite amount of data. For example, take the air temperature outside. At what decimal point does a digital temperature display data? Should the temperature be displayed as 70, 68, 68.1, 68.09 or 68.092 degrees? This is the process of quantization of the input amplitude, rounding it from infinite levels to a finite amount. The other important piece of information is time. The moments at which the temperature is known is reduced from continuous time to a discrete set if the temperature is taken at a uniform rate.

ADCs perform both these tasks. The resolution or accuracy of an ADC determines the precision with which the input is rounded in amplitude. Sampling speed or update frequency of an ADC sets how fast the digital output is refreshed. An example of quantization is shown in Figure 2.1. An arbitrary input signal is quantized over 8-levels at a rate of δT. Increasing either the resolution or reducing T_s increases the accuracy of the estimation of the input signal. Increasing either the sampling frequency or resolution comes at the cost of power consumption and area of the circuitry. ADC designers seek to increase resolution and sampling frequency with minimal increases in area and power.

The accuracy with which an ADC can determine an input signal is referred to as its resolution. It is often specified by a number of levels (M) or bits (N). For

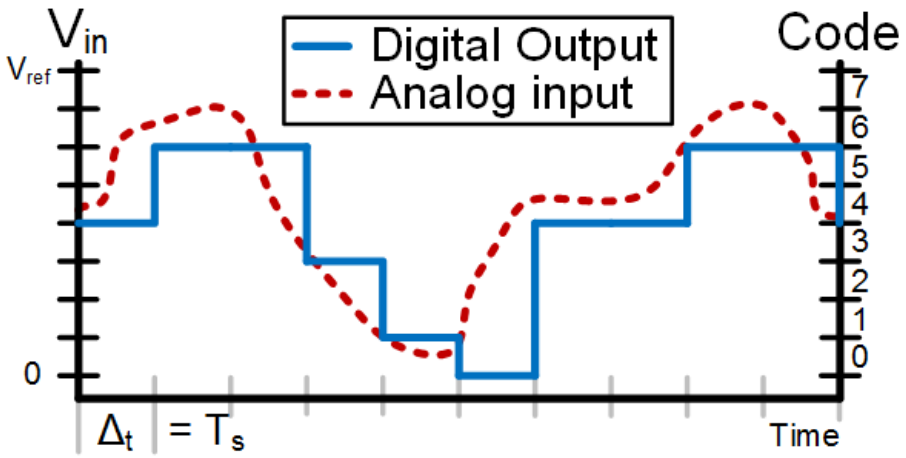


Figure 2.1: This is a demonstration of quantization performed by analog-to-digital converters. The input is rounded to one of 8 levels.

every one bit of resolution, the number of levels increases exponentially (2.1).

$$M = 2^N \tag{2.1}$$

It is used in combination with an external reference (V_{ref}) to determine the input range of the ADC. The difference between two adjacent levels in ADC is referred to as the least-significant bit (LSB). The LSB in voltage (V_{LSB}) of an ADC can be calculated (2.2). For an N-Bit resolution ADC the errors present in the ADC less than $V_{LSB}/2$ [2](2.3).

$$V_{LSB} = \frac{V_{ref}}{M} \tag{2.2}$$

$$V_{err} = \frac{V_{LSB}}{2} \tag{2.3}$$

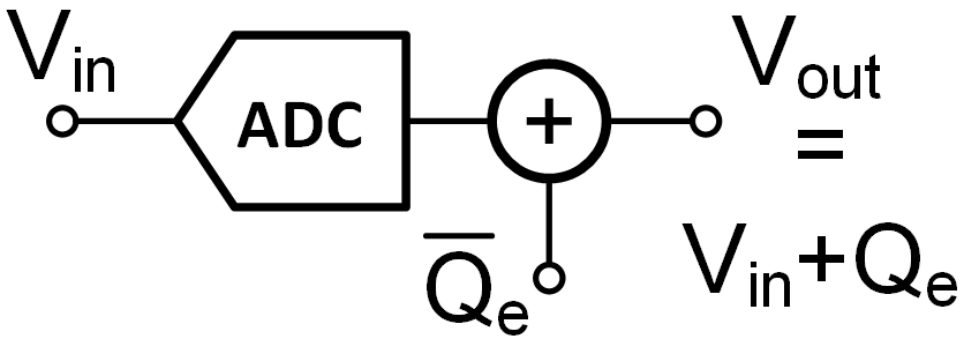


Figure 2.2: This is a model of a generalized ADC with quantization noise modeled as an additive noise source after quantization.

Sampling frequency (F_S) is defined by how often a new version of the input signal is quantized by the ADC, and the digital output becomes valid. The difference between two sampling instances is referred to as the sampling period T_S. Nyquist theorem determines the usable bandwidth to $F_S/2$ [3]. There is a class of ADCs referred to as oversampling ADCs who trade off bandwidth for other performance benefits [4]. Oversampling ADCs are not focused on in this dissertation, but the switched-capacitor ring amplifiers can be applied to those designs.

With finite sampling frequency and resolution, an ideal ADC will always result in a loss of information due to quantization. This is referred to as quantization noise or error (Q_e). It can be modeled as an additive source occurring in series with the ADC seen in Figure 2.2. Quantization noise can modeled as a white noise source [5]. A white-noise noise implies that the noise density across frequency is constant. The quantization noise power can be calculated with (2.4). The output of an ADC can be modeled as the V_{in} + Q_e.

$$\overline{P}_{qe} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.4}$$

Quantization noise power can be reduced decreasing the V_{LSB}, which requires increasing the resolution if the same input range is desired. A useful term to define is signal-to-quantization-noise ratio (SQNR) with respect to a full-scale sinewave. Full-scale refers to the peak-to-peak voltage of an input sinewave being equal to V_{ref}. From there, the expected ideal dynamic performance with a full-scale input can be determined by (2.5).

$$SQNR_{ideal}[dB] = 6.02 * N + 1.76 \tag{2.5}$$

Outside of quantization noise, other factors will degrade the performance of an ADC. They can be categorized into distortion and noise. Distortion is the non-linear deviation of the ADC's transfer function away from an ideal straight line. This often results in harmonic spurs in the output frequency spectrum of the ADC. Noise is added to the input signal by the active devices used to process it. Noise can degrade the accuracy of a single sample but can be mitigated by averaging the output. A dynamic performance measurement captures these effects and is called signal-to-noise-distortion ratio (SNDR). It is defined as the ratio of the signal power to all other sources (device noise,quantization noise, distortion). Peak SNDR of an ADC is used to define an effective number of bits (ENOB) (2.6) in the presence of an dynamic input.

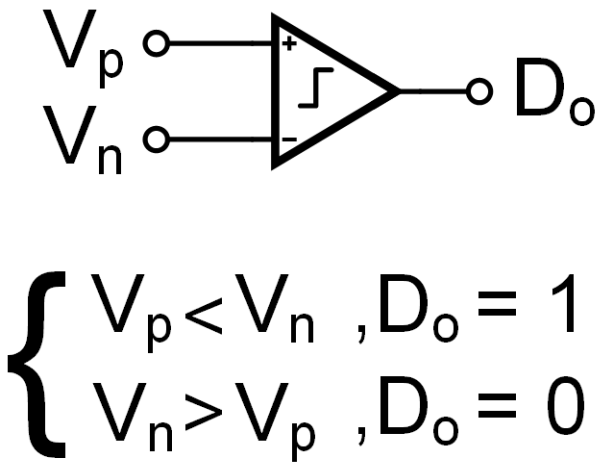


Figure 2.3: A circuit diagram of a comparator and its ideal input-output transfer function are shown

$$ENOB = \frac{SNDR_{PEAK} - 1.76}{6.02} \tag{2.6}$$

Now that some basics of ADCs have been covered, a few example architectures will be summarized leading to the pipelined ADC. The pipelined ADC will lead to the design of residue amplifiers of which ring amplifiers perform efficiently.

2.2.1 Comparator

The symbol for a comparator can be seen in Figure 2.3. A comparator outputs a digital signal representing the difference between the terminals. A high or 1 signal is expected when the positive terminal is higher than the negative. A low

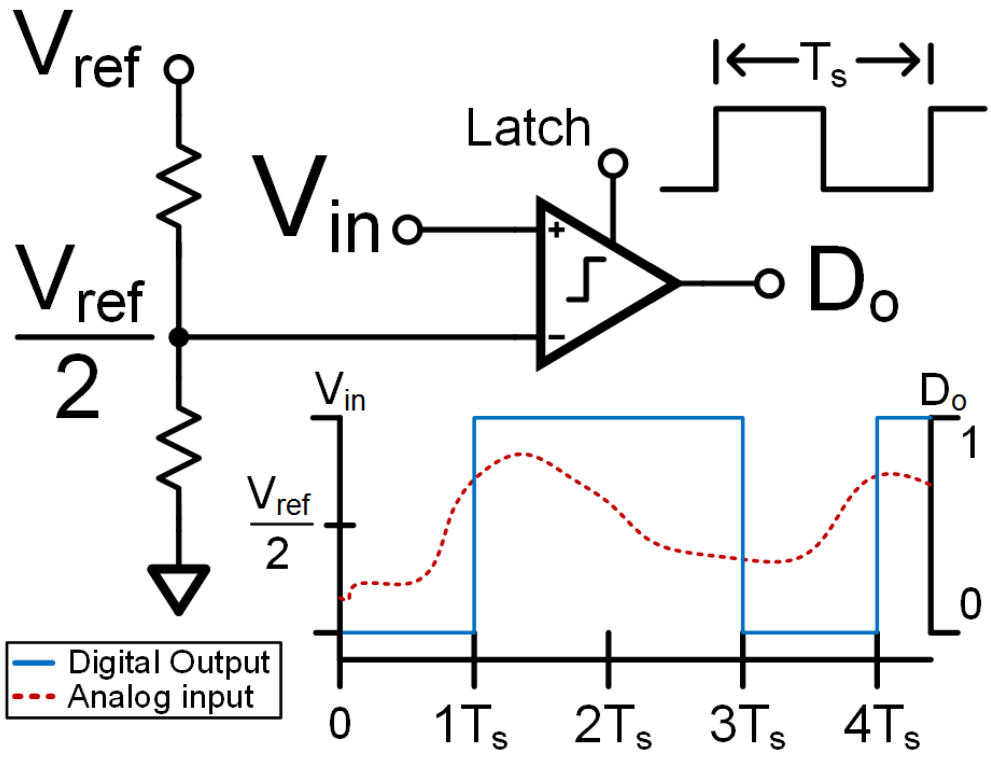


Figure 2.4: Shown is a comparator configured as a one bit ADC with a resistor ladder providing the reference threshold.

or 0 signal is expected when the opposite condition occurs at the input of the comparator. This dissertation primarily uses latched or clocked comparators [6] which only provide a valid comparison after the rising edge of the clock signal.

A comparator's non-idealities include offset errors. An offset moves the comparison trip point of the input nodes away from zero. This can result in an error when comparators are used for quantization. The offset resulting from threshold mismatch of the input devices is determined by (2.7). To reduce the offset of the comparator by two, it requires a four times increase in the size of the input devices.

$$\Delta_{TH} = \frac{V_{th}}{sqrt(W_i * L_i)} \tag{2.7}$$

A comparator can be used as a one-bit ADC, as seen in Figure 2.4. A reference is applied to one terminal through a resistor ladder. The output is valid at the rising edge of the clock signal (Period = T_s). The one bit output is the digital estimate of the input signal. This structure offers limited performance due to the low resolution.

2.2.2 Flash ADC

A solution to get higher resolution is to use a flash ADC [7]. A flash ADC can be seen in Figure 2.5. The structure consists of parallel comparators that latch at the same instance. The references used by the comparators must be a space by V_{LSB} for proper conversion. Resistor-ladders are used to create the equally spaced references.

The number of comparators required is equal to the number of levels (2.1) in the ADC minus 1. Therefore, the number of comparators increases exponentially with resolution. For high resolution applications, the number of comparators required becomes untenable due to power and area constraints. Non-ideal effects also exasperate this effect. The maximum input referred error of an ADC must be less than a half an LSB (2.3). The offset of the comparator appears directly at the input. The offset of all the comparators in the flash-ADC must be less than half an LSB. Increasing resolution also puts a stringent requirement on the

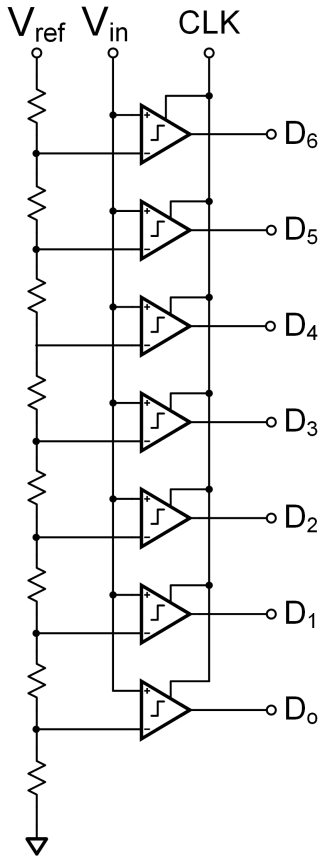


Figure 2.5: A simplified schematic of an 3 bit flash analog-to-digital converter is shown. This figure includes the 7 references generated by a resistor ladder and 7 comparators to achieve 3 bit resolution.

comparators themselves. The input devices must be large which also requires an increase in power and area. The offset can be cancelled with circuit design [8], but flash-ADCs are still limited at higher resolutions due to the sheer number of comparators needed.

There exist other ADC architectures that remove this limitation of a large number of precise comparators. Successive-approximation register (SAR) ADCs

instead apply a search algorithm to determine the input signal [9]. A singular comparator is used. A comparison is made. Depending on the result, a digital-to-analog converter (DAC) updates the reference voltage to the comparator. Generally binary-search algorithms are employed. Depending on the application, signal-dependent algorithms can achieve higher efficiency [10]. While a SAR relaxes the requirement on the number of comparators to one, it requires the comparator be clocked sequentially.

2.2.3 Sub-ranging ADC

A sub-ranging ADC is another ADC architecture that attempts to overcome flash ADC limitations [11]. An example of a two-step sub-ranging ADC can bee seen in Figure 2.6. It consists of two ADC_{sub}, a DAC, and a subtractor. Sub-ranging ADCs work in a sequential manner. First, a ADC_{sub} will quantize the input. Then, an analog-recreation of the digital output is subtracted from the input signal. That result is passed to another ADC_{sub}, which is then quantized. This works because the digital output of the first-ADC contains the input signal V_{in} plus the quantization error $\mathrm{Q}_{E,1}$. When the analog recreation of that digital output is subtracted from the input only $\mathrm{Q}_{E,1}$ remains to be processed by the succeeding ADC_sub. The backend ADC_{sub}'s digital output of a two-stage sub-ranging ADC contains the quantization error of both ADC's 2.8. When the two digital outputs are combined, only the quantization error of the backend ADC_{sub} remains. The overall resolution of a sub-ranging ADC is sum of the resolution of all the ADC_{sub}.

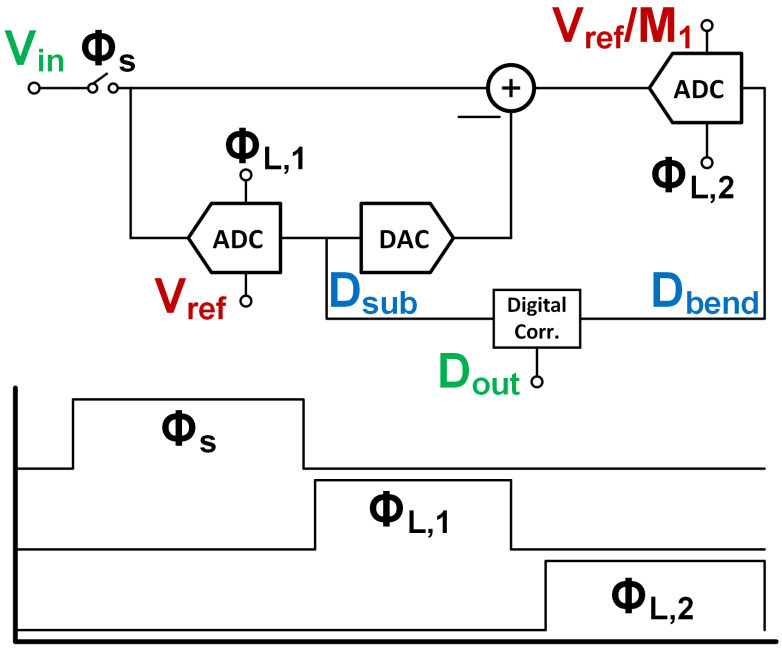


Figure 2.6: A two-stage simplified system level diagram of a sub-ranging ADC is shown. After the input is sampled and quantized by the first ADC, the quantization error is sent to a another ADC which further reduces the overall quantization error of the ADC.

$$D_{bend} = Q_{E,1} + Q_{E,2} \tag{2.8}$$

This dramatically reduces the number of comparators required. A 10-bit flash ADC would require 511 comparators. A sub-ranging ADC with two 5-bit flash ADC requires only 30 comparators! However, the backend ADC_{sub} needs a V_{ref} scaled by a factor M to function properly. M is the number of levels in the preceding quantizers of the sub-ranging ADC. Therefore, the LSB of the backend ADC_{sub} is as small as the overall LSB of the entire ADC. This leads to inefficiency as the input devices of the backend comparators must be large. While this uses more

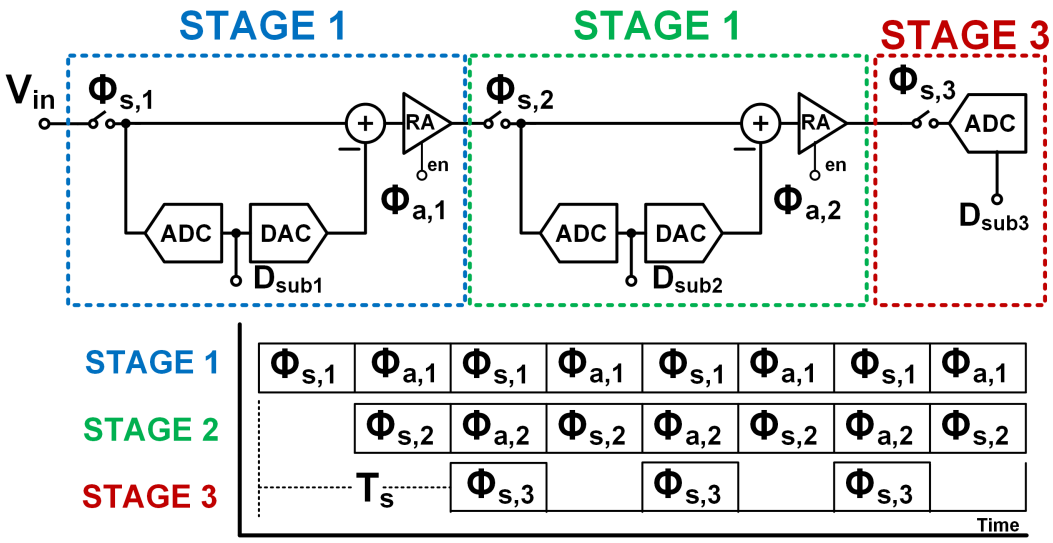


Figure 2.7: This is a system level and timing diagram of a three-stage pipelined ADC.

comparators than SAR ADC, it can be operated at a higher speed. The two-ADCs can be run in parallel allowing for conversion times to approach that of a flash-ADC. For very high resolutions, the accuracy requirements of the backend comparators become a limiting design factor. A pipelined ADC can be used to overcome that limitation.

2.2.4 Pipelined ADC

A pipelined ADC can be seen in Figure 2.7. A pipelined ADC shares many similarities with a sub-ranging ADC. Similar to a sub-ranging ADC, a pipelined ADC passes the residue of a prior conversion to either another pipelined stage or a back-end ADC. Unlike a sub-ranging ADC, the residue passes through a gain stage [12].

This gain stage preforms residue amplification (RA). By amplifying the residue, the succeeding ADC_{sub} can use a full-scale reference instead of a scaled one. Without the scaled reference, the ADC_{sub}s are only required to be as accucrate as their resolution. The closed-loop gain of the residue amplifier ($G_{CL,RA}$) is related to the number of levels (M_sub) in the preceding ADC_{sub}. Setting $G_{CL,RA}$ equal to M_sub will amplify the residue to occupy the entire full-scale reference.

Generally, a pipelined ADC stage's operation can be broken up into two distinct phases. One occurs when a new signal is sampled and quantized (Φ_s), and the other when the residue is amplified (Φ_a). A pipelined ADC's namesake comes from the timing of individual stages relative to each other. In an intermediary pipeline stage, while sampling (Φ_s), the stage samples amplified residue of the preceeding stage. During amplification (Φ_a), the succeeding stage is sampling the amplified residue of this stage. The conversion time of a pipelined ADC is defined by the sampling and amplification process.

Pipelined ADCs can achieve high precision while achieving faster conversion speeds than a comparable resolution SAR. A pipelined ADC will update its digital output at the same rate that it takes a single stage to perform its two operations. However, all pipeline stages must process a sample before the digital output is valid. This results in output latency of a few clock cycles (T_s). Whether latency is important depends on the application in which the ADC is used. If timing of each phase is assumed to be a 50 % duty-clyced version of the sampling clock, the ADC conversion time is dominated by the longer of these two operations. Because flash ADCs can be used as the ADC_{sub} of pipeline stages, the overall conversion

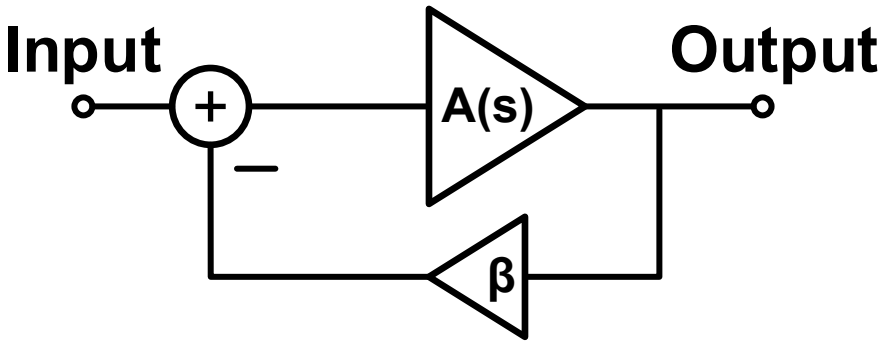


Figure 2.8: This is a system level diagram of a generalized negative feedback system used to achieve.

time is usually determined by the time needed by residue amplifier.

Therefore, the residue amplifiers of a pipelined ADC are critical to the overall performance. Significant errors relative to the resolution of the ADC introduced by the residue amplifier will degrade overall performance. In addition, the residue amplifiers often are the single most power consuming block of the pipelined ADC. Implementing efficient residue amplification will directly lead to efficient pipelined ADC implementations. How residue amplification is accomplished with switched-capacitor circuits and OpAmps is covered in the next section.

2.3 Residue Amplification

Any deviation away from the ideal gain of the residue amplifiers will degrade the ADC's transfer function. Achieving precise gain in the presence of process, voltage, and temperature variations (PVT) associated with fabrication of circuits is not an easy task. One way to accurately perform is to used a high-gain amplifier in

negative feedback (Figure 2.8. With sufficient gain in the forward path (A(s)), the gain will approach $1/\beta$ [13]. β is created by the ratio of two like elements (resistors or capacitors) which exhibit good matching characteristics in the presence of PVT variations. Because ADCs are inherently a sampled system, switched-capacitor amplification circuits are a natural fit [14].

2.3.1 Switched-Capacitor Amplifiers

A two-phase switched-capacitor amplifier can be seen in Figure 2.9. In one phase (Φ_s), the input is sampled onto the capacitor C_S, and the feedback capactior (C_F) is reset of its previous value. In the next phase (Φ_a), charge transfer is performed moving all the charge from C_S to C_F. The resulting closed-loop gain of this structure is (2.9).

$$A_{CL} = \frac{C_S}{C_F} \tag{2.9}$$

The matching of these capacitors will affect performance of the amplifier, but this section and dissertation focuses on the errors introduced by the amplifier. The amplifier in negative feedback can be implemented by an OpAmp. The open loop response, A(s), of a single-pole OpAmp is describe in (2.10). A_{DC} is the DC gain of the OpAmp, and w_p is a left-half plane pole.

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{w_p}} \tag{2.10}$$

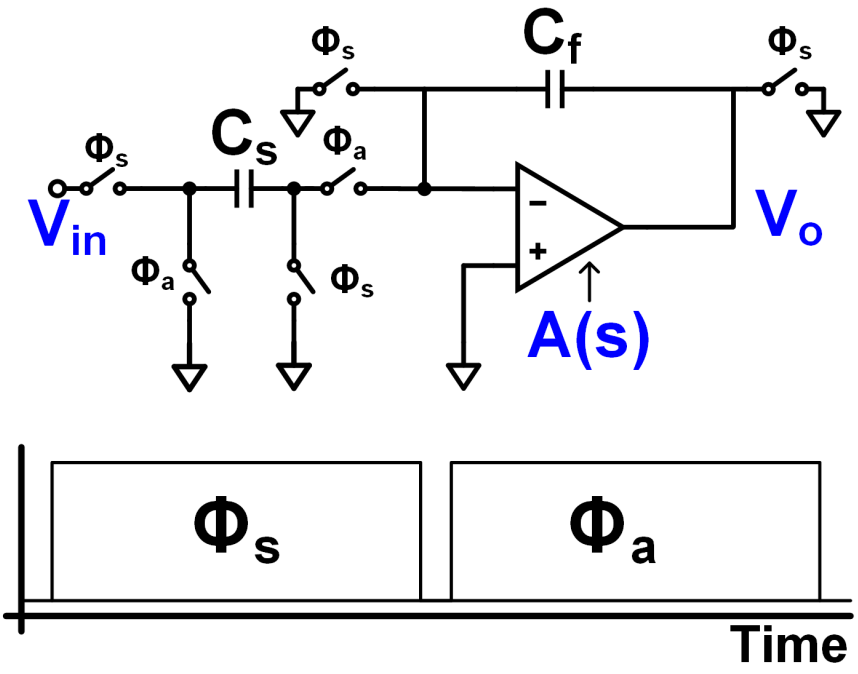


Figure 2.9: Seen is a a switched-capacitor gain stage circuit and timing diagrams. A high-gain amplifier is configured in negative feedback to achieve a precision gain value.

An amplification error can be expected if A(s) does not have infinite bandwidth and gain. A switched-capacitor amplifiers amplification error can be separated into two pieces, static (E_s) and dynamic error (E_d). The E_s is defined as the difference between the ideal output and the settled output when the amplifier has been given an infinite amount of time to settle (2.11). E_d is the difference between the instantaneous output at time T and when it is have been given an infinite amount of time to settle (2.12).

$$E_s = Output_{Ideal} - Output(\infty) \tag{2.11}$$

$$E_d = Output(\infty) - Output(T) \tag{2.12}$$

The E_s caused by the OpAmp is described by (2.13). E_s is a function of DC properities (A_{DC}) of the OpAmp not the frequency response. This error is caused by the non-zero voltage at the V_G due to finite gain. This prevents the complete discharge of C_s. In contrast to the E_s, the E_d due to the OpAmp is determined by its bandwidth not A_{DC}. For a single-pole step-response, the E_d is (2.14). τ refers to the time-constant (in radians) of the amplifiers closed-loop bandwidth.

$$E_s = \frac{1}{1 + \beta A_{DC}} \approx \frac{1}{\beta A_{DC}} \tag{2.13}$$

$$E_d = e^{-t_s/\tau} \tag{2.14}$$

β in these equation is feedback-factor of the switched-capacitor amplification circuit. It is determined by the capacitive divider back to the input of the OpAmp (2.15). C_{IN} refers to the input capacitance of the amplifier. It further reduces the feedback factor, but does not affect the ideal closed-loop gain (2.9) of switched-capacitor amplification circuit. Reducing β increases both E_d & E_s. E_d is increased because loop bandwidth is proportionally related to β. Increasing the closed-loop gain (2.9) results in a decreased β. Because the closed-loop gain is proportionally related the resolution of the first-stage, amplifier non-idealities are in part determined by system level design of the pipelined ADC.

$$\beta = \frac{C_F}{C_S + C_F + C_{IN}} \tag{2.15}$$

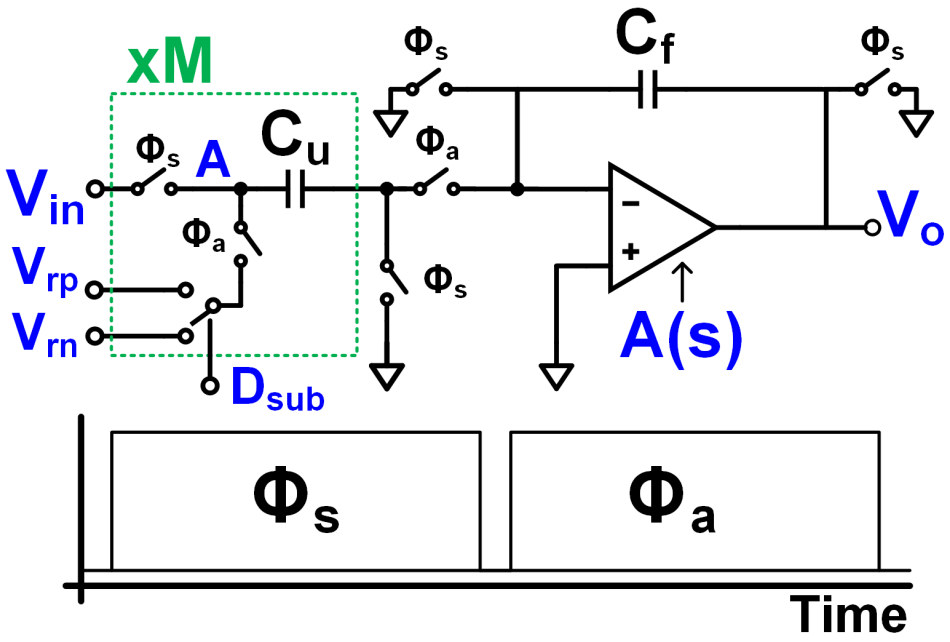


Figure 2.10: A multiplying digital-to-analog converter switched-capacitor circuit is presented. In the sampling phase (Φ_s), the input signal is sampled onto M unit capacitors. In the amplification phase (Φ_a), the capacitors are switched respective to D_{sub} to create the quantization error and amplify it.

2.3.2 Residue Amplifiers for Pipelined ADCs

Two distinct actions need to occur for proper residue amplification; one is to create the residue, and the other is, of course, amplification. The circuit in Figure 2.9 is modified so that during Φ_A, node A of C_S is changed from an analog ground to a analog recreation of the input-signal quantized by the ADC_{sub}. This creates a voltage of V_{in}-V_{DAC} across the sampling capacitor which is amplified by the closed-loop transfer function (2.9).

A circuit implementation of this can be seen in Figure 2.10. It is referred

to as the multiplying-digital-to-analog converter (MDAC)]. C_S is separated into M capacitors C_u of equal magnitude. During amplification, node A of the unit capacitors is switched to either V_{rp} or V_{rn} depending on the digital input (D_{sub}). D_{sub} comes from the ADC_{sub} of the pipeline stage. In this configuration, the Q_e of the ADC_{sub} is amplified.

Errors are introduced during the process due to the finite bandwidth and gain of the amplifier in feedback. The contribution of this error to the overall ADC is best analyzed by referring the error to the input of the ADC. As described earlier, these errors can be analyzed at the output of the amplifier and broken into E_s and E_d. For the first residue amplifier, the gain value is simply the $G_{cl,ra}$ of that stage. For succeeding stages, it is the product of closed-loop gain of all prior residue amplifiers. Due to this effect, the first-stage residue amplifier's errors are the most critical.

OpAmps are traditionally used as the high-gain amplifiers in negative feedback in the MDAC. If a single-pole OpAmp is assumed, the prior error analysis is used (Section 2.3.1) to determine performance requirements of the OpAmp in terms of A_{DC} and frequency response (τ). As noted earlier, feedback factor directly impacts the magnitude of amplification errors. Feedback factor is also directly related to the choice of resolution in the ADC_{sub}. It is reasonable to assume requirements of the OpAmp are also influenced by that design choice.

E_s of the OpAmp will first be analyzed to understand the DC gain requirement in a Pipelined ADC with M levels. This can be demonstrated by input referring the static-gain error (2.13) of the amplifier (2.16). $G_{CL,RA}$ is equal to (2.9) where

C_s = M*C_u.

$$E_s, ir \approx \frac{1}{\beta * A_{DC} * G_{CL,RA}} \tag{2.16}$$

By setting (2.16) equal (2.2), an expression for the required DC gain of the OpAmp can be expressed normalized to a reference voltage of 1.

$$A_{DC} = \frac{2 * M}{G_{CL,RA} * \beta} \approx 2 * M * \frac{C_S}{C_F} * \frac{C_S + C_F}{C_F} \tag{2.17}$$

Input capacitance (C_{IN}) of the amplifier is omitted from this analysis in (2.15). The residue amplifier will need an open-loop gain approximately twice that number of levels. As the closed-loop gain ($G_{CL,RA}$) of the residue amplifier increases, the product of β and $G_{CL,RA}$ trends towards one [15]. Required DC gain is insensitive to the choice in ADC_{sub} resolution. Another factor not accounted for is redundancy in the MDAC, used to relax the offset requirement of the ADC_{sub} comparators [16], but it has a negligible effect of the trend with stage resolution. The overall result is that high resolution pipelined ADCs need high-gain amplifiers in order to have no degraded performance.

For high-resolution pipelined ADCs, high gain OpAmps are needed. CMOS scaling trends have not been universally beneficial to analog circuits. In terms of speed, the circuit devices have improved, but key parameters relating to gain have not. Intrinsic gain of MOSFETs ($g_m * r_o$) has reduced. A typically solution to address this involves cascoding gain stages in the amplifier. However, supply voltage has decreased to lower power, but threshold voltage (V_{TH}) has not making

it impractical to cascode. All these factors have made high-resolution OpAmps based ADCs increasingly inefficient to design in deep sub-micron process compared to other ADC architectures. Pipelined ADC implementations have still continued in sub-micron processes. Some of the solutions designers have found to overcome OpAmp limitations are summarized in the following section.

2.4 Prior work in Pipelined Analog-to-Digital Converters

Pipelined ADC's traits of high-to-medium resolution and moderately high conversion speeds are still desirable in sub-micron technologies. This section provides a brief overview of recent trends in pipelined ADCs. They are focused on to overcoming OpAmp implementation issues due to scaling. A common-theme among the trends is to take advantage of scaling trends instead of designing circuits that are harmed.

2.4.1 Calibrating Amplifier Errors

One way to correct errors in ADC is through calibration [17]. ADCs are inherently attractive for calibration as their outputs are digital in nature. Scaling trends have only made digital circuits more efficient. Principally calibration requires detection of these errors. Figure 2.11 shows the input-output transfer function of an MDAC similiar to the one Figure 2.10. Finite DC gain causes the slope of the transfer function ($G_{CL,RA}$) to deviate from it's ideal value. This can be digitally corrected

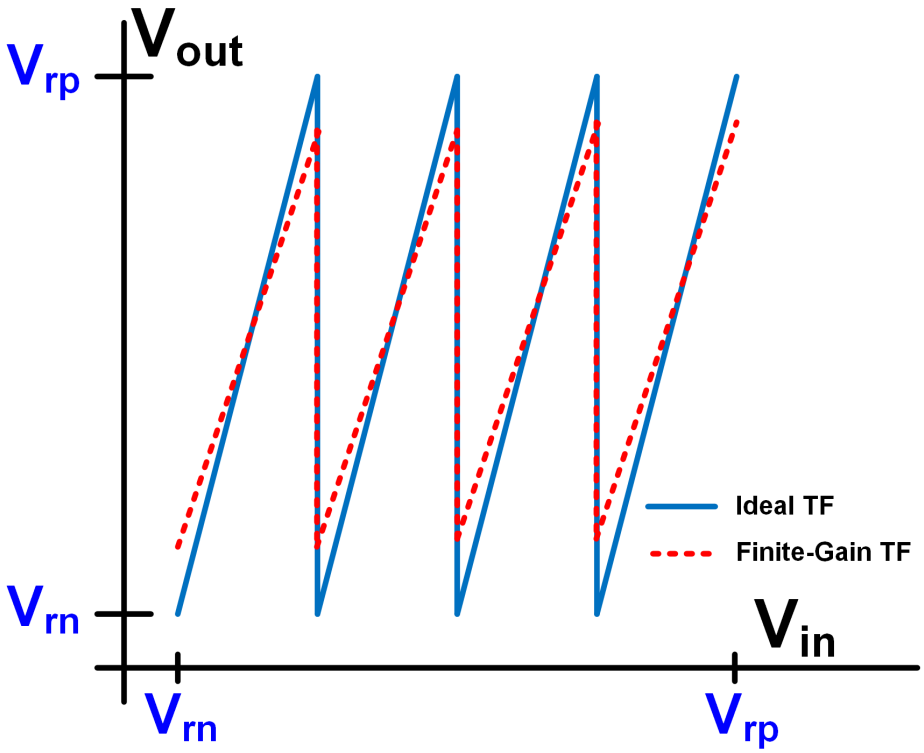


Figure 2.11: A graph of the an ideal 4 level pipeline stage transfer function and the same transfer function when the operational amplifier in the stage has finite-gain limitations

by altering the radix associated with the pipeline stage to its correct value [18].

One way to calibrate is to use foreground calibration with a known input signal and measure the code errors [19]. However, this requires interrupting the normal operation of the ADC if these calibration schemes want to track errors that change over time. Background calibration instead processes both the test signal and input signal at the same time [18,20]. This concept can be applied even further by using non-traditional amplifiers used in an open loop configuration [21].

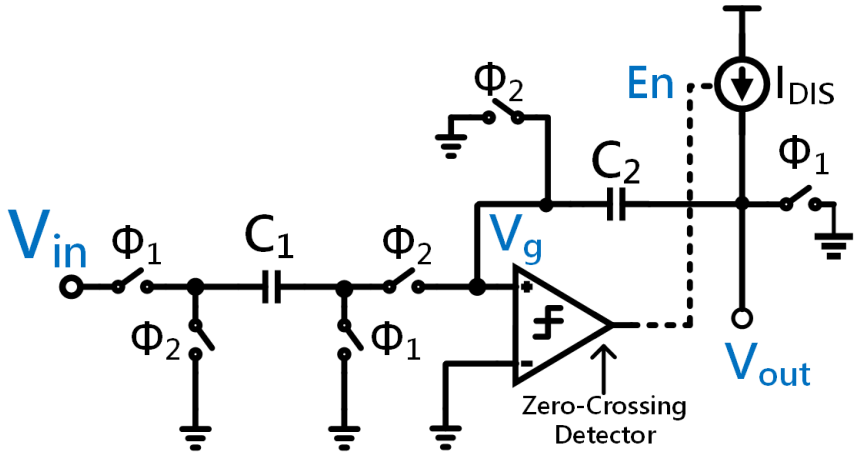


Figure 2.12: This is a circuit diagram of a zero-crossing base detector. The discharge-current source is turned off when the virtual ground crosses the threshold.

2.4.2 Zero-Crossing Based Circuits

Zero-crossing based circuits are another technique used to overcome process-scaling limitations [22]. The main principle is to replace an OpAmp in the MDAC with a comparator. A zero-crossing based implementation can be seen in Figure 2.12. The desire is to set the voltage across the sampling capacitor to 0. This is the same condition at the end of charge transfer amplification in a SC amplification circuit. This results in the correct voltage across the feedback capacitor. A zero-crossing based detector determines when the node V_x reaches 0 and stops discharging the output.

Incorrect amplification results in a non-zero voltage across the sampling capacitor. This can occur due to an incorrect discharge rate, comparator delay, and other factors [23]. One advantage of zero-crossing based circuits is that they can

operate at very low voltages due to requiring very little head room [24]. Achieving high precision with them is possible when combined with a traditional telescopic OpAmp [25].

2.4.3 Alternative Amplifiers and Amplification Structures

Other techniques have involved removing or altering the OpAmp itself. One of those technique is the digital amplifier [26]. It borrows similar techniques from zero-crossing based circuits, but instead uses a capacitive DAC on the output of an OpAmp to drive the virtual ground-to-zero. This circuit assists the OpAmp with digital circuitry. Another implementation of this architecture uses no OpAmp and instead uses a DAC to drive a difference of a input voltage and DAC to zero [27].

Other techniques include using dynamic amplifiers that offer additional advantages over an OpAmp. Some of those implement increased bandwidth and slew current only during certain moments of amplification. This allows for increased settling performance with minimized static power [28]. A dynamic source-follower was used as a residue amplifier in [29]. Gain in these circuits becomes dependent on transistor parameters such as the values of intrinsic capacitance. Many of the implementations revolve around the use of deep sub-micron timing and calibration over heads [30]. This allows dynamic amplifiers to achieve higher resolutions.

Another approach is to improve the circuits where OpAmp are used. Through the use of switched-capacitor techniques, the performance of an OpAmp can be improved. One technique is correlated-double sampling [31, 32]. It offers a reduction

in offset and 1/f noise of the amplifier while also reducing the error due to finite gain of the OpAmp. Another switched-capacitor circuit technique is correlated-level shifting [33]. By sampling an estimate of the output and placing it in series with the OpAmp, loop-gain during amplification is increased. Another benefit is relaxing of required amplifier output swing.

Of course there is always the approach of building better amplifiers. One OpAmp replacement to emerge is called the ring amplifier [34]. It is intended to replace operational amplifiers. A very simple inverter based ring amplifier can be seen in Figure 3.1. It consists of three-cascaded gain stages allowing for high DC gain to be achieved in sub-micron processes. This allows pipelined ADC designs to be created without the inherent need for calibration normally associated with these smaller geometries. The biasing and structure of the ring amplifier gives it dynamic characteristics during amplification. The overall result is that during the initial moments of amplification, the ring amplifier exhibits increased slewing capability and bandwidth. This allows for very efficient residue amplification. The next chapter will describe ring amplifier functionality and how their design differs and is similar to OpAmps.

Chapter 3: Ring Amplifier Operation and Theory

High-performance and efficient amplification is a critical part of pipelined ADCs. To relax circuit requirements of analog-to-digital converters (ADC), residue amplification is performed in pipelined ADCs. Traditionally, operation amplifiers (OpAmp) have been used to perform residue amplification. Scaling trends have had a negative effect on OpAmp design and efficiency. Despite this trend, it is still possible to build high-performance SC amplifiers due to the recent development of ring amplifiers [34]. A inverter based ring amplifier is seen Fig 3.1. They are three-stage uncompensated amplifiers that possess a dominant pole at their output.

Ring amplifiers have been used as residue amplifiers in many high performance data-converters in recent publications [34–41]. The purpose of this chapter is to discuss ring amplifier settling performance and how it differs from OpAmps. Biasing of a ring amplifier will be covered. Small-signal analysis of ring amplifiers will be explained. Large-signal effects during amplification result in dynamic biasing. The dynamic biasing results in improved settling performance versus what is predicted by small-signal analysis. A design example is presented between a ring amplifier and a single-pole OpAmp to demonstrate this effect. Prior work in ring amplifiers and how they have change system level design of pipelined ADCs is covered in Section 3.4.

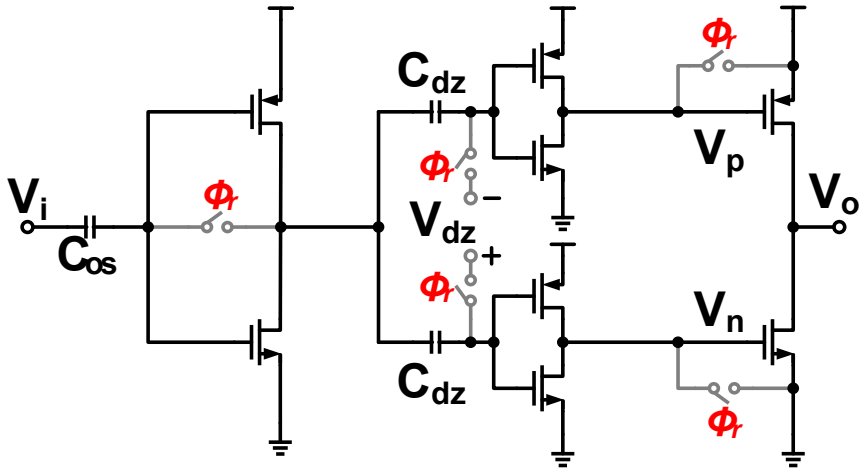


Figure 3.1: A single-ended inverter based ring amplifier used to amplification in a pseudo-differential MDAC.

3.1 Ring Amplifier Biasing and Operation

This section explains how biasing of a ring amplifier's stage is done. A differential current-starved inverter ring amplifier will be used as an example. It is seen in Figure 3.2. One of the output paths is omitted from the diagram for clarity. More detail on these ring amplifiers is in Chapters 4, and 5.

3.1.1 Current-Starved Inverter Ring Amplifier Biasing

It is easiest to explain the biasing of a ring amplifier starting from the output stage. The output stage is a common-feature across all ring amplifiers. The output quiescent current is by set by the gate voltages (V_p & V_n) of the PMOS and NMOS output transistors. It's important to note that the biasing node is also the signal input node of this stage. In other words, a ring amplifier output stage has both

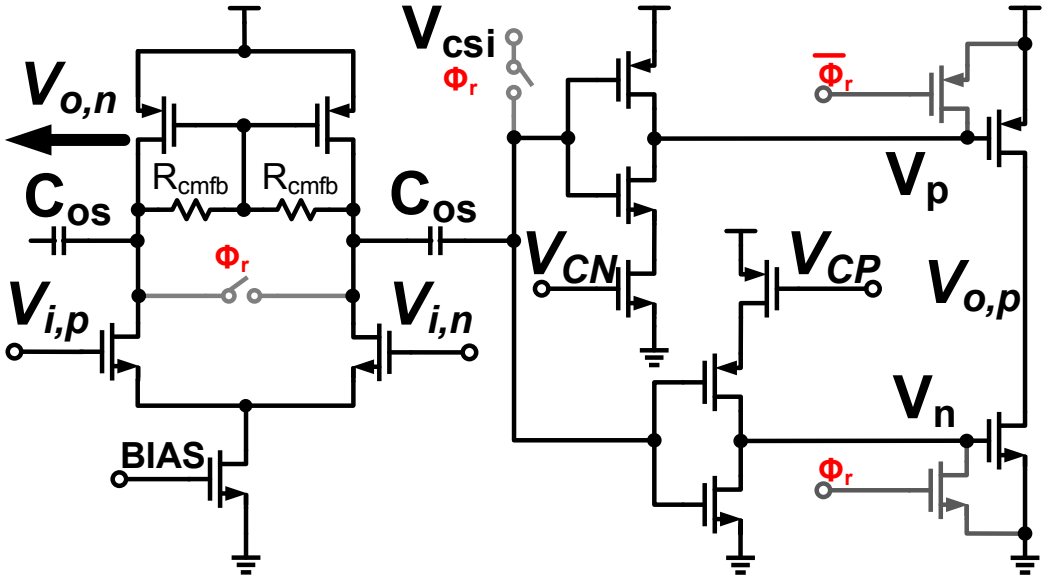


Figure 3.2: This is a differential input current-starved inverter ring amplifier used to discuss ring amplifier biasing and operation. The second and third stages of the negative output $V_{o,n}$ path are not shown for figure clarity.

the bias and signal on the same input nodes. As will be explained in Section 3.2.2, allowing the bias of the output stages to vary enables the ring amplifiers to exhibit dynamic bandwidth characteristics that can improve settling performance. The static bias of the output-stage should be nominally set to a small current. This output stage will serve as the dominant pole of the amplifier. Biasing of the output-stage of the ring amplifiers is often referred to as creating a "deadzone". Deadzone refers to a large-signal effect that will be covered later.

From a small-signal perspective, a ring amplifier obtains a dominant pole at the output through the biasing of the output stage into a low transconductance state. In the CSI ring amplifier, the output is biased through the nodes V_{CN} and V_{CP}. The bias of the output-stage is created from the structure of the second

stage. The output transconductance (gm_3) can be set in this way.

The second-stage must also be biased correctly. Similar to how the bias of the third stage is performed by the second stage, the bias for the second stage is applied through the level-shifting cap C_{os} of the first stage. The current-starved inverters of the second stage can be thought of as inverters with variable trip points. The trip point is adjusted by changing V_{CN} and V_{CP}. If the bias (V_{csi}) is not correct, the output-stage biasing will be compromised. For example, if V_{csi} is moved towards V_{dd} away from the nominal value, the output bias nodes (V_p & V_n) will be moved closer to V_{ss}. The output PMOS device will turn on more. A low transconductance output-stage is no longer valid and may result in instability.

V_{csi} can be generated through a replica bias circuit. A current-starved inverters "default" operational state is defined to be when the gate voltage applied to controlling (or tail) MOSFET is maximum. For NMOS and PMOS transistors, this is V_{dd} and V_{ss} respectively. The two current-starved inverters in second stage do not have the same device sizes. Therefore, the trigger points are different even when they are biased to the default state. The nominal trigger point of this second stage is created by taking a replica of the second stage inverters in parallel with a diode connection as seen in Fig 5.9 in Chapter 5.

The slewing capability of the ring amplifier is determined by the physical size of the output devices. To estimate the maximum slew capability of a ring amplifier, apply a rail-to-rail signal at the gate of the devices and measure the drain-source current. Matching the NMOS and PMOS slewing currents helps to reduce common-mode errors that arise during amplification. Increasing slew current can

result in either quicker settling or instability. When the output stage devices are made larger, they load the second stage more significantly which may require additional power consumption of the second stage for stabilization.

The first stage of the CSI ring amplifier in Fig. 3.2 is NMOS input differential pair with a current-source. A common-mode voltage is set through the resistors (R_{cmfb}). This bias point is saved across the level-shifting capacitors (C_{os}). In addition, this also provides an auto-zeroing effect. The noise performance of ring amplifiers will be explored later in Chapter 4. The output common-mode of the ring amplifier in this example will be set by a slow integration loop seen in Fig 5.9. It replaces the direct V_{CN} bias, and instead sets the control voltage properly so that the sampled output common-mode to V_{cm}. This is further elaborated on in Chapter 5

The CSI ring amplifier is not the best, per se, but serves as an example for explaining ring amplifier small-signal and large-signal characteristics.

3.1.2 Current-Starved Inverter ring amplifier Small-Signal Analysis

It is important to state that the small-signal approximation is only accurate when the input of the ring amplifier ($V_{i,p}$ and $V_{i,n}$) is near zero. In switched-capacitor circuits, this condition occurs at the end of amplification. Analyzing the small-signal performance of the ring amplifier gives insight into the behavior near the end of settling. This helps estimate the overall settling performance but does not tell the whole story. As will be detailed in Section 3.2.2, dynamic effects occur

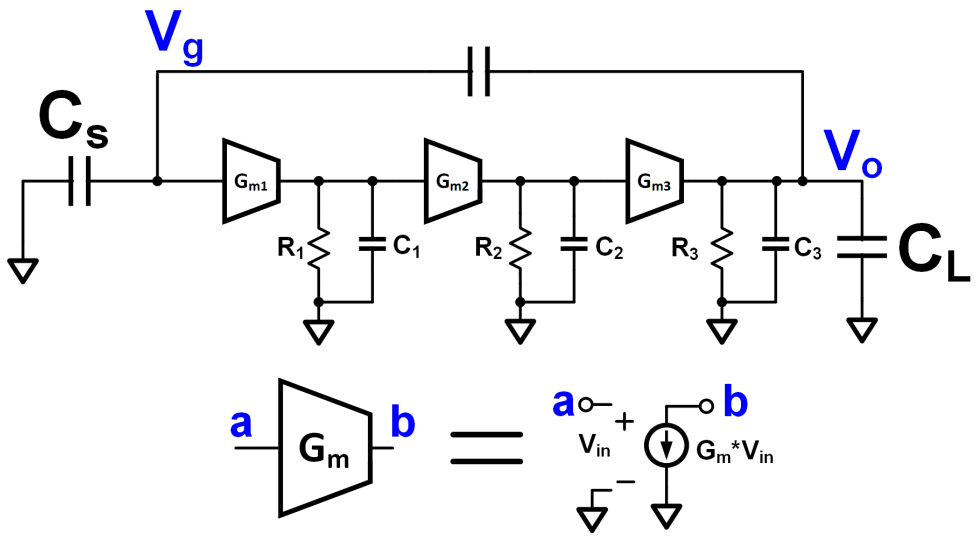


Figure 3.3: A simple linearized small-signal model of a ring amplifier during swithced-capacitor amplification is shown. Each gain stage of the ring amplifier is assumed to consists of a transconductance block, resistor and capacitor.

during the beginning and middle of their settling action that can lead to either increased settling performance (desired) or oscillations (undesired).

Having an understanding of ring amplifier small-signal characteristics allows a designer to make better design decisions. The large-signal response of ring amplifiers requires iterative design to ensure proper functionality. Many times the same circuit improvements to small-signal performance will boost large-signal performance. The small-signal characteristics can also be used as a comparison point with OpAmp based implementations.

One way to analyze a ring amplifiers, small-signal response is to simplify the structure into a multi-stage cascade of gain stages neglecting the split path to the output. A model representing a ring amplifier in a closed-loop during switched-

capacitor amplification is seen in Figure 3.3. Each stage in the forward path consists of a transconductance element (gm_i), an output resistance (R_i), and capacitance (C_i). In this three-stage ring amplifier, there are three poles. Pole locations are determined by the RC values at each node.

A properly biased ring amplifier has a dominant pole at the output. A dominant pole occurs at a frequency much lower than the other non-dominant poles. The first two or interior stages are responsible for the non-dominant poles.

$C_{1,2}$ come isintrinsic loading of the devices in stage 1 and 2, the loading of the next stages 2 and 3, and layout parasitics that result from circuit realization. $R_{1,2}$ are primarily determined by the devices in stages 1 and 2. In a switched-capacitor circuit the output load is capacative. Therefore, the output resistance is the determined by the output devices R_3. C_0 is the effective load seen by the output stage (3.1). C_3 is the intrinsic capacitance of the output devices. C_L is the output load (next stage sampling). C_F and C_S are the sampling and feedback capacitance of the amplification stage. C_{IN} represents the input capacitance of the amplifier and any stray capacitance to ground from layout parasitics.

$$C_0 = C_3 + C_L + \frac{C_F * (C_S + C_{IN})}{C_F + C_S + C_{IN}} \tag{3.1}$$

In medium and high resolution switched-capacitor ADC applications, C_L, C_S, C_F are determined by noise budgeting in the ADC, not amplifier optimization. Increasing the capacitance lowers the generated sampling, or kT/C noise. Thus these capacitors tend to be orders of magnitude larger than $C_{1,2,3}$. This helps

ensure a dominant pole located at the output. The three poles ($W_{1,2}$, W_{DP}), in radians, are determined to be (3.2) and (3.3) respectively.

$$\omega_{1,2} = \frac{1}{R_{1,2} * C_{1,2}} \tag{3.2}$$

$$\omega_{DP} = \frac{1}{R_3 * C_O} \tag{3.3}$$

Under the assumption that $\omega_{1,2}$ exist at a frequency higher than the unity gain bandwidth (ω_{UGBW}), ω_{UGBW} can be calculated by taking the small-signal gain-bandwidth product (3.4). The open-loop gain of a ring amplifier is given by (3.5).

$$\omega_{UGBW} = \frac{gm_1 * R_1 * gm_2 * R_2 * gm_3}{C_O} \tag{3.4}$$

$$A_{DC} = -1 * gm_1 * R_1 * gm_2 * R_2 * gm_3 * R_3 \tag{3.5}$$

With the feedback factor (β) (3.6), the loop unity-gain bandwidth (ω_{LBW}) (3.7) can be calculated.

$$\beta = \frac{C_F}{C_F + C_S + C_{IN}} \tag{3.6}$$

$$\omega_{LBW} = \beta * \omega_{UGBW} \tag{3.7}$$

While ring amplifiers can achieve large bandwidths due to the boosting of gm_3 by the gain of the first two stages (A_1,A_2), this can also lend itself to increased variation across process, temperature and voltage (PVT) variations. Controlling multiple parameters simultaneously requires novel and efficient circuit design. In addition, the non-dominant poles, $w_{1,2}$, are also determined by device parameters and are susceptible to process variations (PVT). These non-dominant poles can degrade the phase margin of the loop if they are too close to unity-gain bandwidth. Ring amplifier biasing is also heavily dependent on the exact threshold voltage (V_{th}) of MOSFETs. V_{th} is also PVT dependent which can cause issue without proper biasing circuits.

Small-signal analysis shows that ring amplifiers are heavily technology dependent and PVT variant. This does not appear to be a high performance amplification structure. Just evaluating a ring amplifier through small-signal does not tell the whole story. Large-signal effects give ring amplifiers increased settling performance over traditional static bandwidth OpAmps. These effects are somewhat similar to dynamic amplifier effects [42]. The next section explains how that occurs in a ring amplifier

3.1.3 Current-Starved Inverter Ring Amplifier Dynamic Operation

One important aspect of ring amplifiers is that they do not exhibit beneficial large-signal characteristics unless used properly. Switched-capacitor circuits, Figure 2.9, are one such circuit that results in beneficial dynamic characteristics with ring

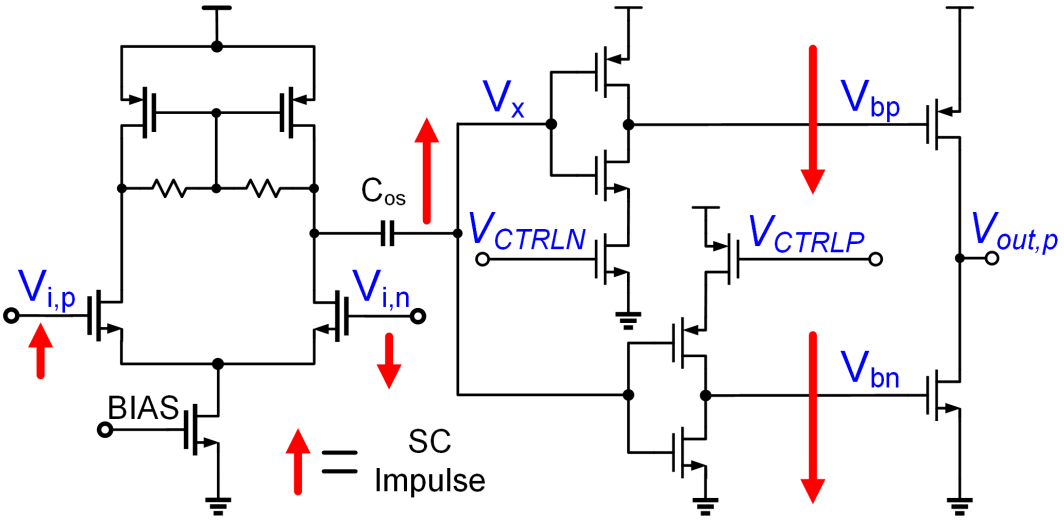


Figure 3.4: Initial impulse directions due to a switched-capacitor input are used to demonstrated how the signal of a ring amplifier can alter the bias of the output stage.

amplifiers. Ideally, the time-varying input seen at the virtual-ground of the amplifier is an impulse. However, band-limiting effects in the switches and amplifiers prevent an impulse from being realized. Regardless of the exact shape and timing of the band-limited signal at the virtual ground when charge transfer is completed, the input at virtual ground is near zero.

When the input is near zero, the small-signal approximations made earlier are valid. It is in the earlier parts of amplifications when the input is non-zero that a ring amplifier exhibits dynamic effects. The input returning-to-zero is important as it provides a reliable condition for a designer to ensure small-signal stability. Without the signal returning-to-zero, the bias of the ring amplifier will be altered. With an altered bias, it is likely the ring amplifier will exhibit excessive ringing or instability.

Bias sensitivity to input voltage may seem like a disadvantage of ring amplifiers, but it is actually critical to ring amplifier settling. In the presence of an input signal, either the NMOS or PMOS in one output path transistor will be biased with an increased gate-source voltage. The other output transistor will be biased with a decreased gate-source voltage. It is this property that allows a ring amplifier to exhibit dynamic effects. The dynamic effects includes a multiplication factor of the output quiescent current that greatly increases slew rate. This magnification factor can easily reach a magnitude of 100 and is dependent on the design. Another effect is increased bandwidth; the increased current through one output transistor results in an increased gm_3. This results in increased small-signal settling performance.

To understand exactly how the dynamic action of a ring amplifier takes place, Figure 3.4 is presented. It shows the direction node voltages take in the presence of an impulse at the input ($V_{i,p}$ & $V_{i,n}$) of a ring amplifier. As can be seen, the V_bp and V_bn move together towards one of the supply rails resulting in the change of bias described earlier. The other differential output channel will show similar behavior but in the opposite direction.

This assumption is confirmed with the simulations seen in Figure 3.5. The output settling response of a ring amplifier during switched-capacitor amplification is seen in Figure 3.5(a). The output rapidly slews and overshoots the ideal output voltage (i.e. 800 mV). A ringing response is seen before the output eventually settles and only E_s remains. E_s is dependent on the small-signal gain of the ring amplifier which is accurately predicted by AC analysis. Insight is gained when the internal nodes of the ring amplifier are observed in Figure 3.5(b). As can be

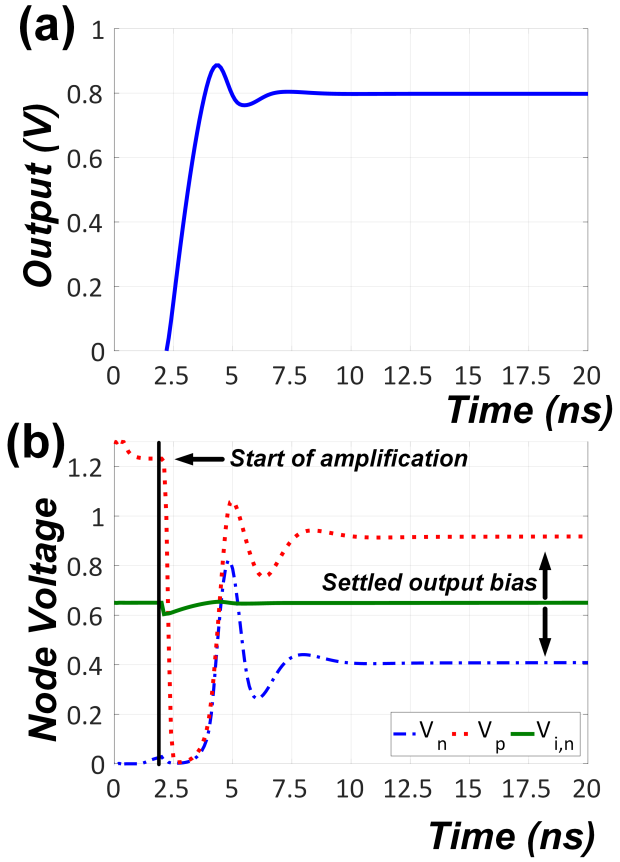


Figure 3.5: Various waveforms of a ring amplifier during switched-capacitor amplification are shown. In (a) the differential output voltage is shown. In (b) the voltage at the gates of the output stage are shown.

seen, the initial impulse at $V_{i,n}$ pushes the output-stage gate voltages dramatically towards the negative rail. The output PMOS is heavily turned on and slewing begins towards the desired output. Eventually, the desired output voltage is overshot. Stabilization then occurs back to the small-signal state. The gate voltages settle to their small-signal bias points seen at the end of amplification. Only one output-path is shown. The other differential path exhibits similar behavior, but

towards the opposite rail.

In this example, designed in 180 nm CMOS, the final settled quiescent current of the differential output stages is 10 μA while the peak differential output current is 1500 μA, due to dynamic biasing. It is difficult to estimate through linear analysis exactly what a given ring amplifiers settling performance will be. However, through large signal transient simulations ring amplifiers, can be compared with OpAmps of similar small-signal bandwidths. This allows a designer to evaluate the increased performance due to dynamic effects.

3.2 Dynamic Bandwidth of Ring Amplifiers

Since the dynamic bandwidth effect is due to large-signal operation, it is hard to quantify through small-signal analysis. This section will describe a testbench and methodology to examine the settling performance of ring amplifiers in comparison with a static bandwidth OpAmp model. This will serve as a design example for how ring amplifiers affect system level ADC design.

3.2.1 Design Methodology

Performance will be measured with transient simulations of the SC gain stage seen in Fig. 3.6. Two different ring amplifiers will be evaluated on of which one has output stage transistors with twice the width. These two ring amplifiers will have their control voltages such that their small-signal bandwidth will be approximately

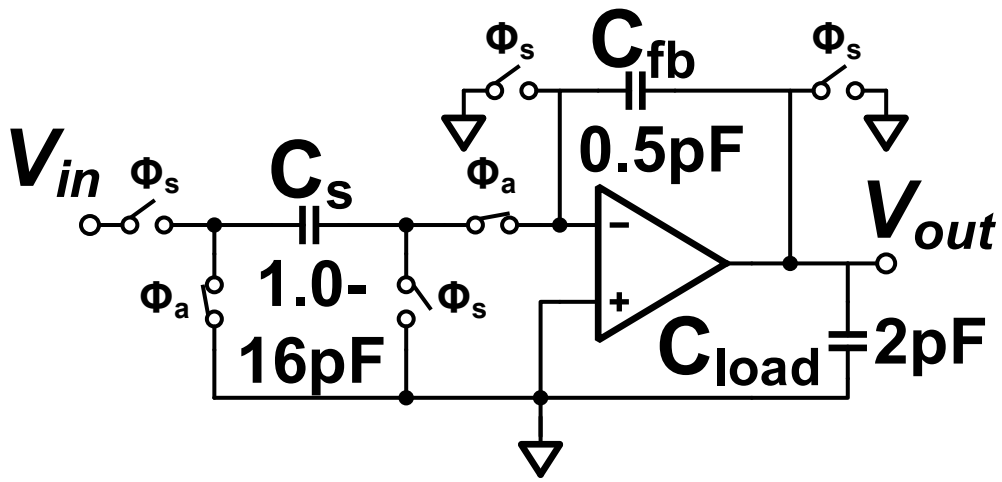


Figure 3.6: Switched-capacitor amplification stage used to investigate dynamic bandwidth of ring amplifiers in comparison with operational amplifiers. C_s is varied to create different closed-loop gains of the structure while minimizing the change in load seen by the amplifier under test.

the same. The sizing of the first two-stages of the ring amplifiers is identical in each case. They are referred to as the 1x and 2x output ring amplifiers.

The performance will be evaluated over different closed loop gains. This will be done by modifying the sampling capacitance (C_S). The load capacitance (C_L), and feedback capacitance (C_{FB}) remain fixed at 2 pF and 500 fF respectively. The closed-loop gains will be 2, 4, 8, 16, and 32 which implies a C_S taking the values of 1, 2, 4, 8, and 16 pF respectively.

Static amplification error (small-signal gain) will not be evaluated in this experiment of dynamic bandwidth. The amplifiers will be said to be finished settling when their E_d reaches within $+/-$ 0.5 percent.

Table 3.1: Loop Bandwidth & Phase Margin of the amplifiers used in the comparison of a OpAmp and Ring Amplifier

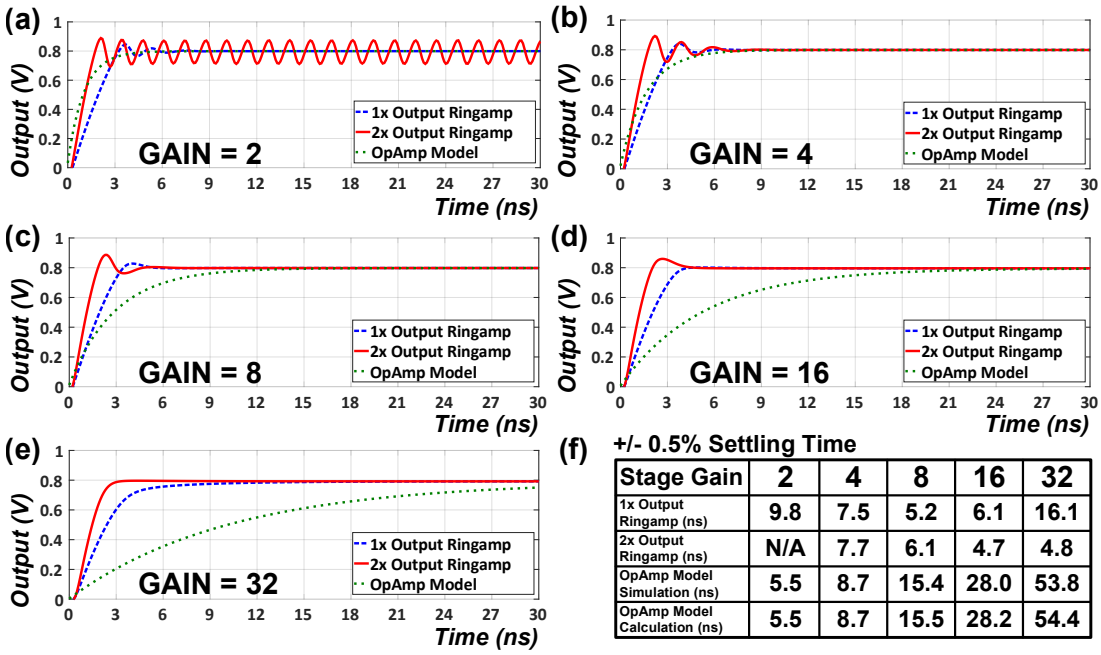
Stage Gain	2	4	8	16	32
1x Output Loop Bandwidth (MHz)	151	95	54	29	15
1x Output Loop Phase Margin (Deg)	61	72	80	85	88
2x Output Loop Bandwidth (MHz)	156	99	56	30	16
2x Output Loop Phase Margin (Deg)	58	69	78	84	88
OpAmp Model Bandwidth (MHz)	153	96	55	29	16

3.2.1.1 OpAmp Model

The results of the ring amplifiers will be compared with an single-pole OpAmp model which has similar loop bandwidth. In order to ensure that the OpAmp model is settling correctly, the +/− 0.5 % will be calculated for all the different loop unity-gain bandwidths (ω_{LBW}) and compared with simulation results. The s-domain transfer function of a one-pole OpAmp in the SC testbench in Fig. 3.6 is given by (3.8). A_{dc} is the amplifiers static gain, β is the feedback factor formed by the capacitive feedback, and w_p is the ω_{LBW} in radians.

$$H(s) = -\frac{C_s}{C_{fb}} \cdot \frac{\beta A_{dc}}{1 + \beta A_{dc}} \cdot \frac{1}{1 + \frac{s}{w_p}} \tag{3.8}$$

The dynamic settling time of a single-pole system is calculated (3.9). T_s is the settling time required, and E_{da} is desired dynamic settling error (0.5 % in this application).



Stage Gain	2	4	8	16	32
1x Output Ringamp (ns)	9.8	7.5	5.2	6.1	16.1
2x Output Ringamp (ns)	N/A	7.7	6.1	4.7	4.8
OpAmp Model Simulation (ns)	5.5	8.7	15.4	28.0	53.8
OpAmp Model Calculation (ns)	5.5	8.7	15.5	28.2	54.4

Figure 3.7: Settling response of two example ring amplifier designs in comparison with the OpAmp model across different closed loop gains (a-e). Experimentally obtained and calculated settling times are summarized in a table (f).

$$T_S = -\frac{1}{w_p} \cdot ln(E_{da}) \tag{3.9}$$

Table 3.1 shows the simulated ω_{LBW} and phase margin of the two ring amplifiers to be evaluated as well as the matched OpAmp models bandwidth.

3.2.2 Dynamic Bandwidth Discussion

All five of the settling responses cases can be seen in Fig. 3.7. The time window of these settling responses increases with stage gain to accommodate OpAmp settling.

In addition, the settling times are summarized in the Fig. 3.7(f). First, the OpAmp model simulation will be evaluated with respect to the small-signal calculation. The OpAmp model behaves as expected with respect to small-signal calculations. When the closed-loop gain is increased, the decreased loop bandwidth results in slower settling times.

In comparison, the ring amplifiers do not follow this trend. Settling times for a particular ring amplifier have minimums that do not correspond with the lowest-stage gain. Starting when the gain is set to two, it is seen that 2x output ring amplifiers oscillates despite having a positive loop phase margin. This shows one of the pitfalls of large-signal systems when only analyzing small-signal parameters. The slewing capability in relation to the delay of the first two stages of the ring amplifier causes oscillation. In the same case, the 1x output ring amp does not oscillate despite only having an extra three-degree of phase margin. However, the slew rate is half of the 2x output case, and thus stabilization occurs during large-signal action.

At lower feedback factors the dynamic bandwidth effect becomes very pronounced. In the gain cases 8, 16, and 32, the slew rate of the ring amplifiers outperforms even the ideal OpAmp models initial settling response demonstrating the dynamic bandwidth effect. Except for the gain case 2, the ring amplifiers out perform the OpAmp model settling due to this effect. The increased slew current allows for a large portion of settling to occur in the initial moments of amplification. Then, once the ring amplifier returns to small-signal behavior, there is a reduced error voltage to settle resulting in increased settling performance compared to a

static bandwidth OpAmp.

In general, the dynamic bandwidth assist becomes more pronounced at higher gains when compared to the OpAmp model. This can be attributed to the fact that the slew capability of the ring amplifier is largely independent of feedback-factor as it is a large-signal characteristic. As closed-loop gain is increased, the relative ratio of slew rate to ω_{LBW} increases. This implies the dynamic bandwidth effect provides a larger assist to the overall settling response. Between the two ring amplifiers, they have different peak performances with respect to closed-loop gain. Increasing the slew rate can provide a larger assist but comes at the cost of decreased stability, resulting from both small and large signal effects which may result in decreased settling performance.

This example is not intended to say that ring amplifiers work best in a particular feedback-factor, or that they are better than OpAmp by a pre-determined amount, but instead is intended to demonstrate how ring amplifier design differs from OpAmps due to dynamic bandwidth. Ring amplifier design is an iterative process where the large-signal slewing capability needs to be balanced with small-signal characteristics, which is where the art of ring amplifier design can be expanded. Ring amplifier designers should look to design methods in control theory and other fields to optimize ring amplifiers.

3.3 Pipelined ADC Design: Ring Amplifiers versus OpAmps

Ring amplifiers and their dynamic bandwidth change how system level design of pipelined ADCs should be approached. A ring amplifier does not necessarily slow down with a lower feedback-factors due to their dynamic bandwidth. As shown in the Chapter 2. a pipelined ADC stage has two phases of operation it must complete within a conversion period. One is Φ_s where sampling plus quantization of the input signal occur, and the other is Φ_a residue amplification. The exact ratio of these two time periods depends on a specific design implementation. A reasonable assumption is that these periods are equal and occupy 50% of the overall sampling period. Whichever of these two operations takes the longest amount of time determines the overall sampling rate of the pipelined ADC.

Another assumption will be made that the amplification time is the dominant of these two. Therefore, the settling speed of the residue amplifier in the first-stage determines the overall conversion speed of the ADC. System level design of a pipelined ADC involves the choice of resolution per stage of ADC_{sub} to achieve the overall required resolution. Resolution of the ADC_{sub} in a pipelined stage directly effects the feedback factor (β) which in directly affects the loop bandwidth as seen in (3.7).

Similar to how the the static error of the OpAmp was analyzed and a derivation for DC gain was found respective to overall accuracy (M) and the choice of ADC$_s ub$ resolution ($\mathrm{G}_{CL,RA}$) in Section 2.4, it will also be done for dynamic error. Ultimately the goal is to relate transconductance (power) to the closed-loop gain of

the residue amplifier and overall resolution. For a single-pole OpAmp, increasing bandwidth by a factor X requires increasing a transconductance by a proportional amount. This requires an increase in static power consumption which degrades the efficiency of the ADC.

First, it is assumed that only dynamic errors will effect the OpAmp performance (2.12). The dynamic error is input referred and set equal to an half an LSB of the ADC (2.3. Then the equation is rearranged equal to the ratio of amplification time (T_a) to loop bandwidth time constant (τ) (3.10).

$$\frac{T_a}{\tau} = ln\frac{G_{CL,RA}}{2 * M} \tag{3.10}$$

Unlike the equation for DC gain, required time-constant settling is not proportionally to $G_{CL,RA}$. For example, if the G_CL of the residue amplifier is increased by a factor of two, the required time-constant settling will decrease by a factor less than two. For further insight we must relate τ to amplifier transconductance. For a single pole OpAmp, τ is equal to $C_0/(gm_1\beta)$. C_0 is the switched-capacitor load, and gm_1 is the first stage transconductance. β is the switched-capacitor feedback factor and is approximately equal to $1/(1+G_{CL})$. The result in 3.10 is then rearranged when τ is substituted resulting in 3.11.

$$\frac{T_a * gm_1}{C_0 * (1 + G_{CL,RA})} = ln\frac{G_{CL,RA}}{2 * M} \tag{3.11}$$

Now the tradeoff of amplifier transconductance for high-resolution pipelined ADC becomes clear. Increasing G_{cl} by a factor of two does relax the ratio of T_a/τ,

but it's by a factor less than two. On the other hand, τ itself is decreased by a factor approximately equal to two. Without changing amplifier topology this would require an increase in power to raise the gm_1 of the OpAmp. Therefore, unlike DC gain of the OpAmp, resolution of a pipelined stage (and therefore closed-loop gain of the residue amplifier) will affect the required gm_1 of the OpAmp. The trend is that a higher-resolution pipeline stage will require a higher power OpAmp.

For a designer of pipelined ADCs with OpAmps, this becomes a limiting trade-off. Increasing stage-resolution requires less pipeline stages to achieve the same resolution which can save power. However, that design decision requires an increase in power of the OpAmps. The overall change in power consumption is hard to predict. It is both technology and architecture dependent, but the trend still holds. Increasing the stage-resolution will eventually result in a extremely power hungry OpAmp. When compared to OpAmps, the benefits of ring amplifiers allow for efficient pipelined ADC implementations. The two important small-signal parameters being DC gain (A_{DC}) and transconductance gm_1.

The three-stage cascaded nature of the ring amplifiers make their innate DC-gain high. The architecture also allows for high output swing even in low-supply voltages associated with modern CMOS technologies. From a bandwidth perspective, the ring amplifier can be designed with less bandwidth than an OpAmp. This is a result of the dynamic bandwidth effects (Section 3.2.2) inherent to the architecture. The large-signal effects ring amplifiers do not follow the same settling trends as OpAmps when β is altered. OpAmps will decrease in speed and require more power to achieve the same settling accuracy. Ring amplifiers may improve in

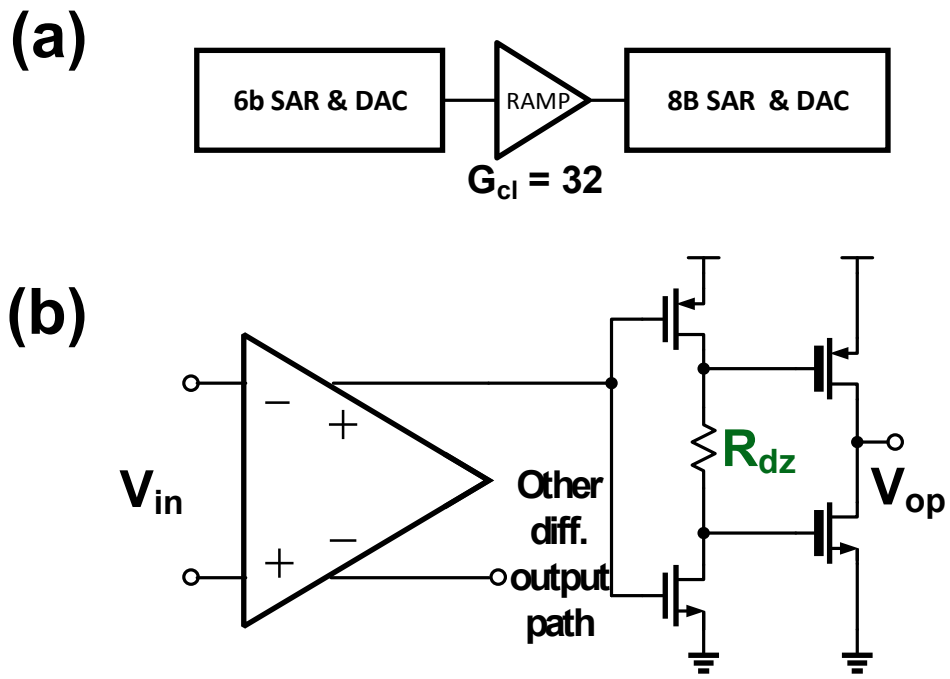


Figure 3.8: A simplified top level diagram of a pipelined-SAR with a ring amplifier (a). The resistor-based output stage of the ring amplifier used in the pipelined-SAR (b).

settling performance as feedback-factor increases.

3.4 Prior Work: Ring Amplifier Pipelined ADCs

The combination of these factors has allowed pipelined ADCs to continue progressing in efficiency despite the trends of process technology. This is best exemplified by pipelined-SAR ADCs using ring amplifiers as a residue amplifier [36, 39]. The general structure of these ADCs is seen Figure 3.8(a). Two medium-resolution SARs are interconnected by a high closed-loop gain residue amplifier. This is implemented with a resistor-based ring amplifier [43] seen in Figure 3.8(b). The ring

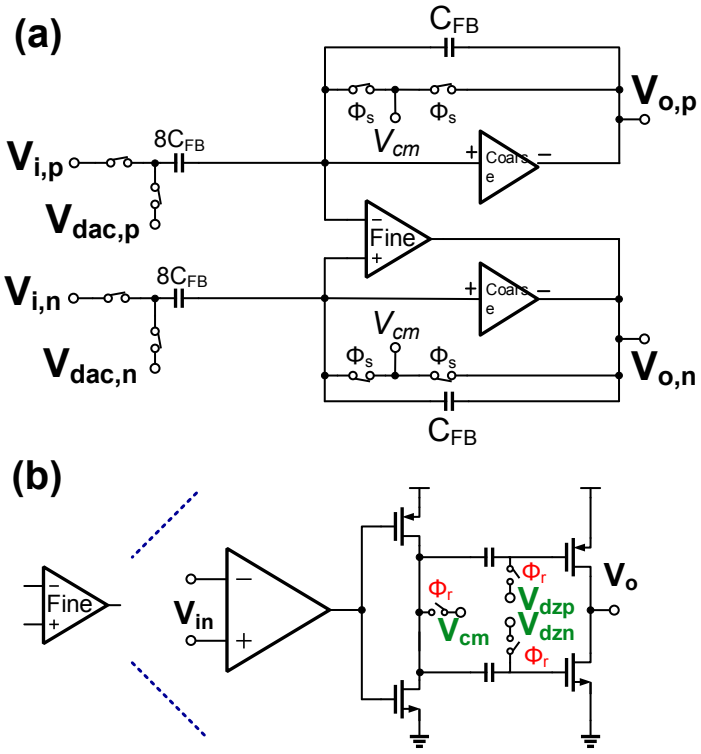


Figure 3.9: The simplified coarse-fine ring amplifier only amplification structure used in (a). The structure the ring amplifier used for fine amplification (b).

amplifiers enable this design by providing highly efficient residue amplification despite the high-gain closed-loop gain of the residue amplifier. The resistor-based ring amplifier biases the output stage through R_{dz}. This allows for a single inverter in the second-stage of the ring amplifier which allows for potential power savings. This ADC design was implemented in 65 nm CMOS and achieved 11.6 bit ENOB at 50 MSPS [36]. The modified version of this architecture in 40 nm CMOS achieved 11.9 bit ENOB at 100 MSPS [39] uses a four-stage ring amplifier.

The coarse inverter-based ring amplifier, Figure 3.1, has been used in a 10.5-bit pipelined ADC [44] as a stand alone residue amplifier. The inverter-based structure

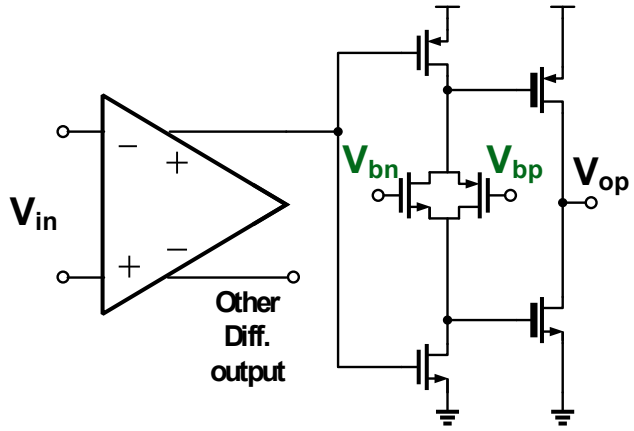


Figure 3.10: Ring amplifier structure used in a 600 MSPS pipelined ADC. The resistors in Figure 3.8(b) have been replaced by biased MOSFET devices.

was best used as a class-B output stage and is difficult to bias for fine settling performance. Two different approaches were developed for higher-accuracy settling performance. The first was to combine the coarse ring amplifier with a correlated level shifting amplification circuit [33]. In the second-phase of amplification, a telescopic OpAmp was used to achieve high accuracy settling [45]. This was furthered refined to coarse/fine amplification structure using only ring amplifiers seen in Figure 3.9(a) [35]. The coarse inverter-based ring amplifiers are designed for initial slewing. After a set amount of time, the coarse ring amplifiers turn off, and a fine single-ended ring amplifier settles the remaining error voltage. The fine ring amplifier embeds its deadzone bias in capacitors after the second-stage seen in Figure 3.9(b). This allows for a less sensitive deadzone voltage as it is not amplified by a second-stage inverter. The output-bias can be correctly set for fine settling. This structure decouples slewing and fine settling performance of ring amplifiers.

The fastest ring amplifier pipelined ADC to date uses a modified resistor based

implementation [38]. The resistor are replaced with CMOS devices in the linear region acting as resistors seen in Figure 3.10. This allows the gate voltage appearing across the output transistor be maximized during slewing as opposed to the resistor in Figure 3.9(b). In addition, the bias at the gate of this deadzone transistors (V_{bn},V_{bp}) can be altered after fabrication. This can be used to change the bias, or with a switching scheme, turn off the second-stage when the amplifier is not used. This pipelined ADC was operated at 600 MSPS and achieved 56.3 dB SNDR due to the use of a ring amplifier in a 28 nm CMOS process.

Other designs have included a multi-path ring amplifier that uses dynamic biasing in one of the paths [40]. One output path uses the second and third stage seen in the Figure 3.8(b) for fine settling. The other output path replaces R_{dz} with a resetable capacitor. This implements a coarse output path the will automatically turn off the output transistors when charge accumulates across the capacitor. Another ring amplifier implementation compensates for stability by adding another pair of resistors to the first-stage inverter [41]. This reduces the effective gain of the first stage and moves the associated pole to higher frequency. Using this technique, a pipelined-SAR ADC achieved 9.5 bit ENOB at 200 MSPS in a 65 nm CMOS process.

Ring amplifiers have provided a new paradigm for designing high-resolution and efficient pipelined ADCs. The following chapters will present two different ring amplifier designs. The first introduces current-starved inverters as a way to bias the output-stage of the ring amplifier in Chapter 4. The other ADC discussed in Chapter 5 further adapts the current-starved inverter structure to allow for

high-precision amplification without affecting minimum settling time.

Chapter 4: Current-Starved Inverter Ring Amplifier and the Noise Investigation Pipelined ADC

4.1 Introduction

This chapter details the design of a 74 dB SNDR Pipelined ADC that use a ring amplifier as the residue amplifiers [37]. This ADC is designed in a 180 nm CMOS process. The ring amplifiers in this pipelined ADC uses current-starved inverters to create the so-called "deadzone" or biasing of the output stage. One of the main objectives of this prototype chip was to investigate the noise performance of ring amplifiers. Previous ring amplifier chips had been limited by sampling noise in the ADC. This chip was designed so that it would be amplifier noise limited, not sampling noise limited. This chip demonstrated that large-signal simulations can estimate the noise performance of ring amplifiers.

This chapter will cover the key features of this prototype pipelined ADC. The first feature is the current-starved inverters used in the second-stage of the pipeline. While briefly introduced in Chapter 3, more detail will be covered here. One of the features of the current-starved inverters is the ability to change the bias or daedzone during amplification. This allows dynamic deadzones to be created. How and why to create dynamic deadzones will be explained. Noise analysis of ring amplifiers will be addressed. Particularly the impact of dynamic bandwidth

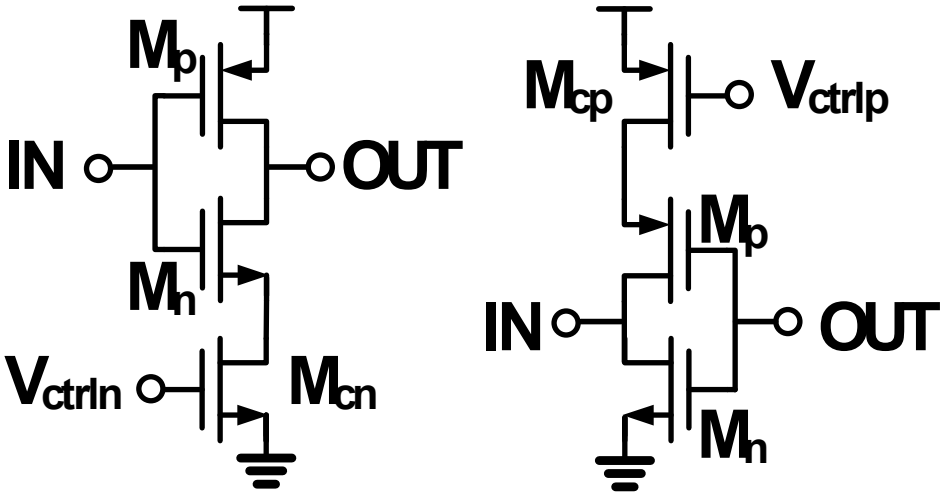


Figure 4.1: Two circuit implementations of a current-starved inverter are shown one with a NMOS control FET and the other with a PMOS control FET

on the final noise performance. The design of the noise investigation pipelined ADC will be presented as well as measurement results from the test chip.

4.2 Current-Starved Inverters

The current-starved inverter (CSI) architecture comes about from the previous capacative deadzone ring amplifiers [34, 35, 45]. Two variations of a current-starved inverter can be seen in Figure 4.1. Using the two current-starved inverter implementations with PMOS and NMOS control inputs, the output stage of a ring amplifier can be biased into the sub-threshold region. They functionally replace the second stage inverters and capacitors in previous ring amplifier design. This saves area as the deadzone capacitors are removed. Another important feature is that they do not need a reset period like capacative deadzone ring amplifiers.

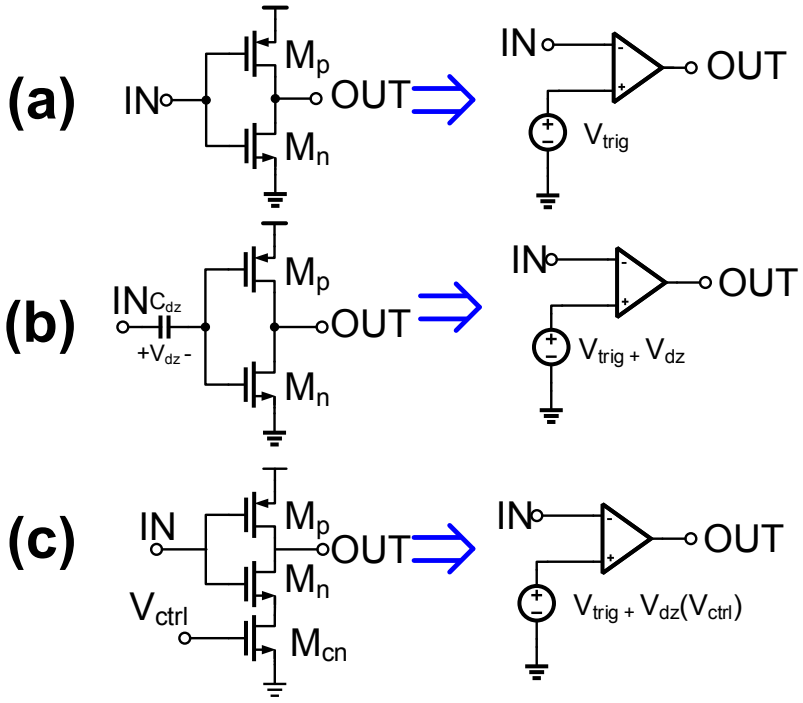


Figure 4.2: Three different inverter implementations and their analogous representation with a differential amplifier.

This also implies that the gate voltage of the control transistors can be altered during amplification. This leads to the development of a dynamic deadzone which is discussed in Section 4.3.

First, the operation of a current-starved inverter will be explained. It makes sense to start from the stand alone inverter seen in Figure 4.2(a). It can be thought of as analogous to a differential input amplifier with a reference on the positive input. The reference voltage is equal to the trigger point of the inverter (V_{trig}). From a digital perspective, the trigger point is the voltage at which the output will flip from a $1 -> 0$ or $0 -> 1$. It can be determined by tying the input and output of the inverter together and measuring the voltage.

An inverter with a capacitor at the input is seen in Figure 4.2(b). Assume that the capacitor has a stored voltage on V_{DZ}. It is very similar to the stand alone inverter case, but now in series with the trigger point is V_{DZ}. Because inverters do not have infinite gain, the output will not rail, allowing a bias to be applied to the gate of the output transistors. Of course, this also implies that the common-mode voltage at the input of this device is very important if an accurate bias is desired.

Finally the current-starved inverter can be seen in Figure 4.2(c). Like the capacitor implementation, the trigger point has a deadzone voltage term. However, this trigger point is now a function of the control voltage. When the absolute value of V_{gs} of the control FET is at its maximum (equal the supply voltage), the current-starving transistor has its smallest resistance and the effect on the trigger point is minimal. This state can be described as the nominal trigger point of the current-starved inverter. As the $|V_{gs}|$ decreases the resistance increases and the trigger point of the inverters is altered. With NMOS control, the inverter trigger point trend is positive. Increasing the trigger point with the same input voltage makes it easier to bias the output voltage closer to the supply due to the inversion of the inverter. PMOS control has the inverse effect of moving the trigger point down, making it easier to bias the output towards ground or the negative rail.

The choice of sizing the two other transistors can effect the overall trigger point range. For example, if the transistors M_{P1} and M_{N1} are matched to M_{P2} and M_{N2} respectively, the resulting trigger points versus $|V_{gs}|$, the control voltage will look like the graph seen in Figure 4.3. When the control voltage is high, the trigger points are virtually identical. Each trace has a notch where the sensitivity to the

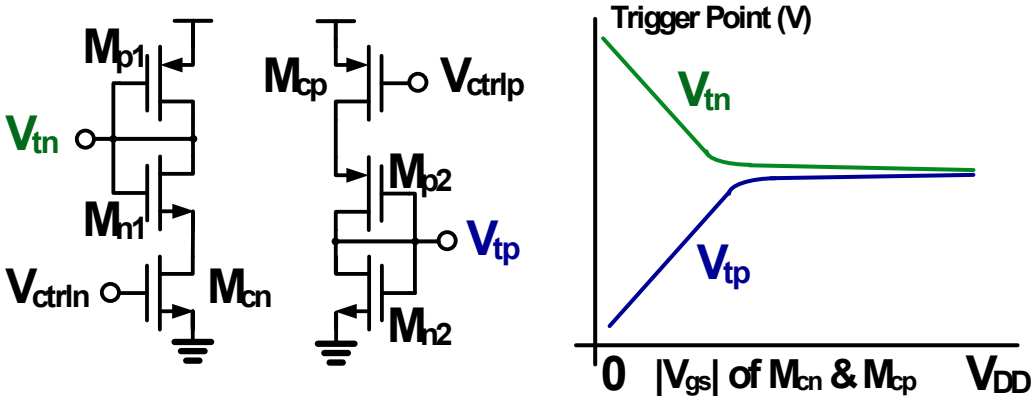


Figure 4.3: Trigger point of two current-starved inverters versus the absolute value of their gate voltages is seen. The variants of the current-starved inverters have either PMOS or NMOS control transistors.

control voltage changes corresponding with the threshold voltage of the control transistors.

Each trigger point trace can be moved vertically by altering the ratio of the NMOS and PMOS transistors to each other. Decreasing the PMOS to NMOS ratio (increasing the relative size of the NMOS) will move the trigger point down, while increasing that ratio will move the trigger point up. This is analogous to adjusting the trigger point of an inverter without a current-starving transistor. It is wise to do this to both paths in a complementary manner. If the second stage inverters to the PMOS output transistor are modified so that the overall trigger point moves up or down, the other current-starved inverter to the NMOS output transistor should be moved in equal magnitude but the inverse direction. This is done to keep the average of the two nominal trigger points.

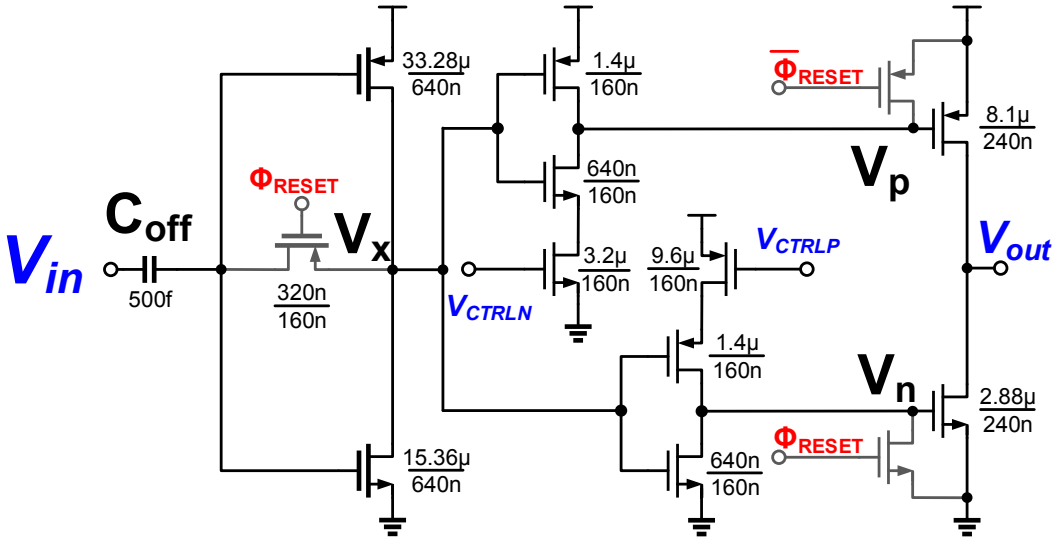


Figure 4.4: Circuit diagram of the psuedo-differential current-starved inverter ring amplifier used in this prototype pipelined ADC. Sizing is shown for amplifier in the first stage of the pipelined ADC.

4.2.1 Current-Starved Inverter Ring Amplifier

The full three-stage current-starved inverter ring amplifier can be seen in Figure 4.4. It is a pseudo-differential amplifier. V_{CTRLN} and V_{CTRLP} set the output current as detailed in Chapter 3. The first stage comprises of an inverter, a switch and a capacitor. As mentioned in the previous section, there is an average nominal trigger ($V_{t,nom}$) point associated with the second stage inverters. By setting V_x equal to $V_{t,nom}$ the output stage is properly biased. Any deviation will cause bias voltages on the gate of the output transistors to be shifted towards either the supply or ground. This error, at best, will only cause the output common-mode to become inaccurate and, at worst, can result in instability and ringing during amplification.

Inverters can be predicted to have an output approximately $V_{dd}/2$ if the input voltage is equal to the trigger point. One approach is to design the first-stage inverter such that its trigger point is equal to the common-mode at V_{in}. If these conditions are met, V_x is assumed to be $V_{dd}/2$. Then the designer should set $V_{t,nom}$ equal to $V_{dd}/2$ by adjusting the values of the PMOS and NMOS transistors of the current-starved inverters. While this condition is sufficient to ensure the output is biased properly, it is hard to ensure across process, variation and temperature (PVT) variatons. That is the function of the offset canceling capacitor and the reset switch.

The variation of the input trigger point away from the common-mode voltage applied at V_{in} can be thought of as an offset. By capturing this offset and removing it from the input, the voltage at the gate of the 1^{ST} stage inverter will be equal to the trigger point. As described previously this will bias the output stage properly and give the ring amplifier its dynamic characteristics. This action is accomplished by C_{OFF} and the NMOS switch transistor controlled by the reset clock (Φ_r).

The voltage across C_{off} is set during the a reset phase. The voltage at V_{in} will be the common-mode voltage V_{cm}. When tying the input and output of the first stage inverter together, the node voltage is equal to the V_{trig}. The voltage stored across the capacitor is equal the difference between the input common-mode voltage and the trigger point that may have change with PVT variations. During amplification, this capacitor level shifts the input signal to the bias to whatever the trigger point is. It also adds an auto-zeroing effect [31]. Node V_x can be expected to properly bias the following stages.

During the reset phase, power can be saved by turning off the second and third stages. Two reset transistors are attached to nodes V_p and V_n. During reset they pull those nodes to V_{dd} and ground respectively. At the same time the control nodes V_{CTRLN} and V_{CTRLP} are set to ground and V_{DD} respectively. This turns off the second stage inverters saving power. The current-starved inverter architecture easily allows the output of the ring amplifier to resemble a high-impedance (Z) output stage.

4.3 Dynamic Deadzone Ring Amplifier

Another feature this prototype chip demonstrated was the introduction of dynamic deadzone control. Dynamic deadzone control means that the bias or deadzone voltage will change during amplification. A ring amplifier naturally has dynamic characteristics. The dynamic deadzone acts as another level of control that allows the dynamic behavior to be influenced by the designer. Altering the deadzone requires changing the voltage across a capacitor or a resistance implementing the deadzone in previous ring amplifiers [34, 43]. Implementing a dynamic deadzone with these circuits requires modifying the circuit to be tunable. One solution would be to implement a bank of capacitors or resistors that are switched during amplification. This will cause a glitch during amplification which can result in degraded linearity of the amplifier.

The current-starved inverter is an attractive design because the bias is set at the gate of a control node. This bias is also not in series with the signal. V_{ctrln} and

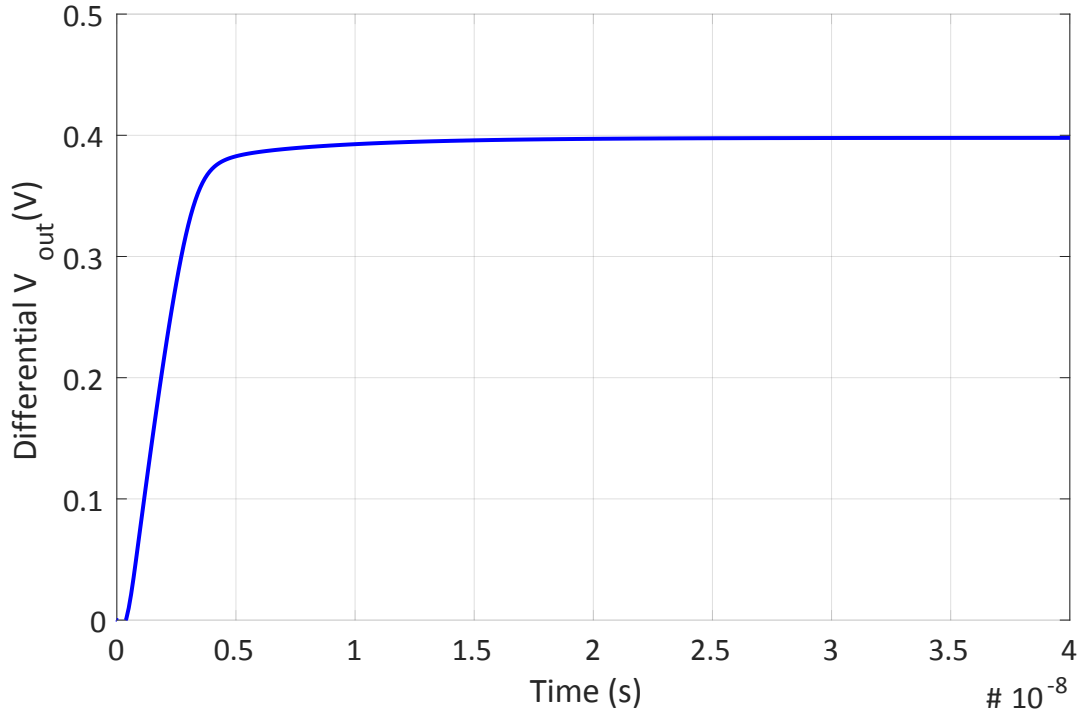


Figure 4.5: This is a settling waveform of an over-damped ring amplifier settling response.

V_{ctrlp}, seen in Figure 4.4, can be altered during amplification without causing a glitch at the output. The dynamic deadzone can be designed in two distinct ways. One would be to design it such that the output bias moves the bandwidth from low $->$ high during amplification. This would correspond with increasing the control voltages ($|V_{gs}|$) during amplification. Controlling the deadzone bias in this manner fights the dynamic characteristics of the ring amplifier which involve a trend in bandwidth from high $->$ low. If the desire is to induce the opposite dynamic behavior of high $->$ low bandwidth, the control voltage should be decreased during amplification.

One might desire to set the bandwidth low in a ring amplifier. However, this

can result in settling behavior that does not exhibit typical ring amplifier settling. This is more likely to occur in ring amplifiers that are already small-signal stable ($\approx$ 90 degree PM). A demonstration of the settling phenomenon is seen in Figure 4.5. This ring amplifier is used in a switched-capacitor circuit with a closed-loop gain of 16. The loop bandwidth is 20 MHz and the loop phase margin is 87 degrees. After the initial slewing, the ring amplifier enters a small-signal amplification state at approximately 4 ns.

The settling response exhibits slewing until the output reaches a critical inflection point and begins to exhibit a one-pole like response. This is desired if it happens close to the desired ideal output voltage, but that does not always occur (i.e. this example). The larger error voltage to be settled by an OpAmp like response increases the amount of time the ring amplifier takes to reduce the dynamic error (E_d).

One way to analyze this large-signal effect is to think of the biasing as creating a deadzone. If the signal spends too much time in this deadzone region, the ring amplifier will likely change to an OpAmp-like response. A low-bandwidth implies a large input-referred deadzone. If the deadzone were kept sufficiently small during the beginning of amplification, and then allowed to increase, the over-damped response can be avoided. This is can be accomplished by a dynamic deadzone that moves the output biasing from a high $->$ low bandwidth during amplification.

Circuitry to accomplish this can be seen in Figure 4.6(a), while the resulting waveforms and timing diagram are shown in Figure 4.6(b). Driving the control nodes of a current-starved inverter ring amplifier is the RC network seen on the

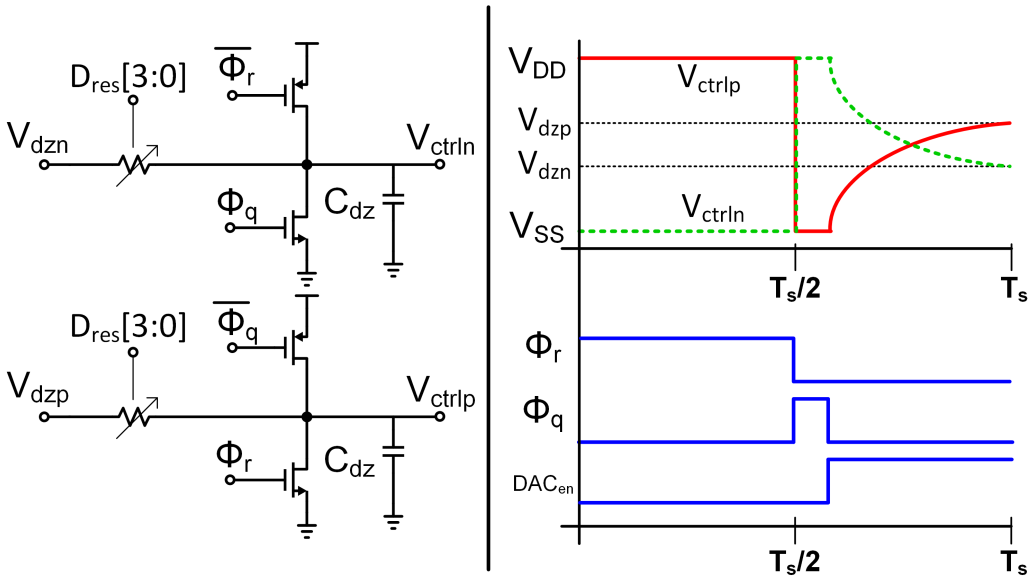


Figure 4.6: This is the circuit diagram used to implement a dynamic deadzone for current-starved inveter ring amplifiers.

left side of figure. During the reset phase of the ring amplifier (Φ_r), V_{ctrln} and V_{ctrlp} are set to GND and V_{DD}, respectively. Φ_q refers to the time immediately prior to amplification; in a pipelined ADC stage this is the time where the ADC_{sub} is quantizing the input. During this time, the ring amplifier is biased into a high-bandwidth state. V_{ctrln} and V_{ctrlp} are set to V_{DD} and GND respectively. This is the initial high bandwidth (small deadzone) condition of the dynamic control.

During amplification (Φ_a), the control node must be brought back to a desired lower bandwidth (high deadzone) control voltage. How this is done and the shape the waveform takes is a design decision. If a linear increase or decrease is desired, a current source could be used charge the capacitor C_{dz}. That would require circuitry to detect when the proper voltage is reached and turn-off the current source. This

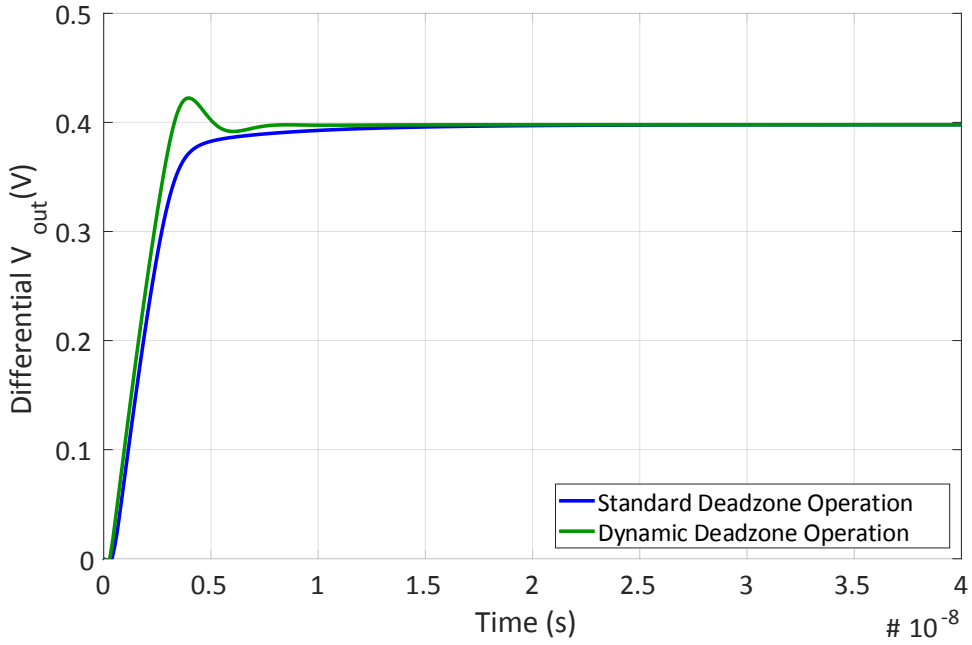


Figure 4.7: This is a settling waveform of an over-damped current-starved inverter ring amplifier with and without a dynamic deadzone enabled.

prototype instead opts for an RC settling approach. While this does not require any additional control circuitry, it does have an initial rate of change greater than a current-source implementation. However, this is unimportant as the sensitivity of the current-starved inverters control node to their trigger point is low when the control voltage is large as seen in Figure 4.3. A digitally controlled resistor is used to account for process variations. When amplification is not occurring, the MOSFETs acting as the resistors digitally switched to a high impedance state.

The effect of the dynamic deadzone can be seen in settle response feature in Figure 4.7. Now the over-damped ring amplifier demonstrates the beneficial large signal characteristics when used with a dynamic deadzone. For a 0.1% E_d, the

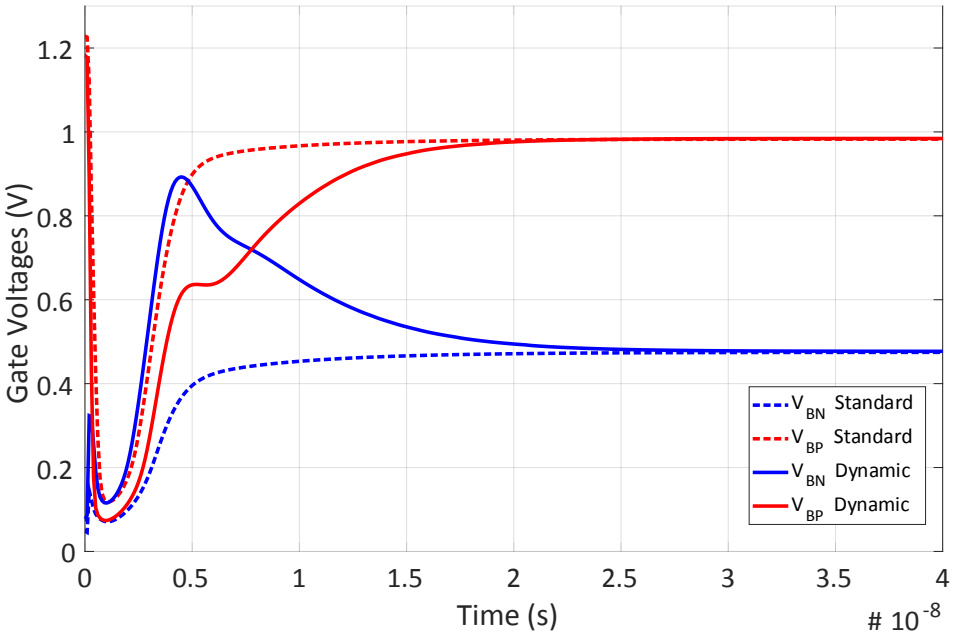


Figure 4.8: This is a waveform of the gate settling voltages of a current-starved inverter ring amplifier with and without dynamic deadzone control.

standard ring amplifier biasing takes 35.7 nS to settle. With the addition of the dynamic deadzone control settling to the same accuracy requires 23.7 nS.

Further insight can be gained for viewing the gate voltages of the ring amplifier with and without the dynamic deadzone. The gate voltages during amplification for both the standard and dynamic mode are shown in Figure 4.8. With the dynamic deadzone the gate voltages stay dip closer to the a supply rail during initial part of amplification. It can be seen that the end of amplification the bias on output stages remains the same. This dynamic deadzone allows low bandwidth ring amplifiers to improve their settling speed.

4.4 Ring-Amplifier White Noise

One goal of this prototype chip was to investigate the noise performance of ring amplifiers and determine if it matches with simulations. As with predicting settling performance, ring amplifier noise performance has both large and small signal characteristics. To estimate the small-signal output-referred integrated-noise ($\overline{V}^2_{O,AMP}$) performance of the ring amplifier, the approach is used from [46]. This involves calculating two quantities: the input-referred noise density of the ring amplifier at the virtual ground ($V_{I,n}(s)$), and closed-loop transfer function $H_{CL,N}(S)$ from the virtual ground to the output. With these two quantities, $\overline{V}^2_{O,AMP}$ can be found by integrating the noise density times the absolute value squared of the transfer function over all frequencies 4.1. Once the output-referred noise of the amplifiers are estimated, they can be input referred to the input of the ADC. This is used in noise budgeting of the top level design of an ADC.

$$\overline{V}^2_{O,AMP} = \int_0^\infty V_{I,n}(f) * |H_{CL,N}(j2\pi f)|^2 df \tag{4.1}$$

A linear model of a ring amplifier in amplification with noise sources added is seen in Figure 4.9. $V_{I,n}(s)$ is the input-referred noise density that will be derived. After this model is used to calculate the $V_{I,n}(s)$, the output integrated noise performance can be calculated. $\mathrm{H}_{CL,N}(S)$ can be assumed to be a one-pole response and is given as such (4.2)

$$H_{CL,N}(S) = \frac{G_0}{1 + s\tau} \tag{4.2}$$

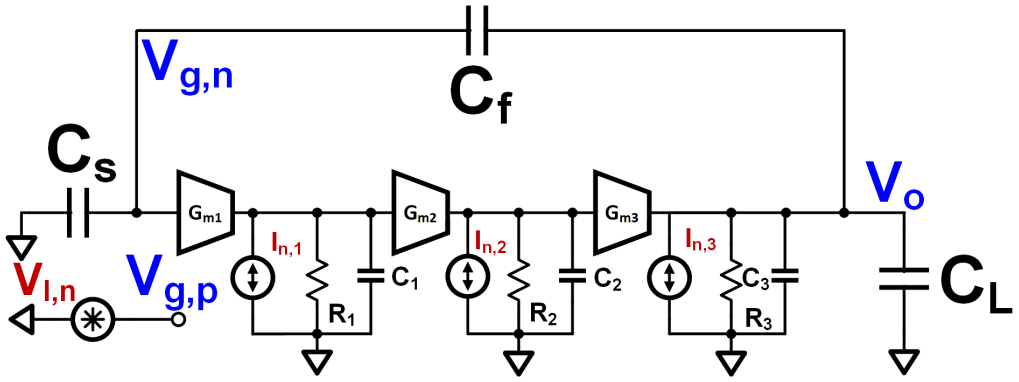


Figure 4.9: A simple linearized small-signal model of a ring amplifier during amplification with device noise sources added. Used to analyze the small-signal noise performance of a ring amplifier.

G_0 is the DC gain of the closed-loop transfer function, and when the A_{DC} of the amplifier is high it is approximately equal to $1/\beta$ or $1+C_s/C_f$. τ is the time-constant of the closed-loop transfer function. It is equivalent to the reciprocal of the loop bandwidth (ω_{lbw}) of the amplifier, which for a ring amplifier is (4.3). C_0 is the equivalent capactive load seen at the output of the amplifier (3.1), which in most cases can be approximated to $C_L+C_f*C_s/(C_s+C_f)$.

$$\omega_{lbw} = \beta * \frac{gm_1 * R_1 * gm_2 * R_2 * gm_3}{C_O} \tag{4.3}$$

$V_{I,n}(s)$ can be found by finding the output-referred noise density and input-referring it by the squared A_{DC} of the ring amplifier. In Figure 4.9 each stage of the ring amplifier has a noise-current ($I_{n,i}$). It is equivalent to a MOSFET operating in strong inversions noise current. This noise is white with infinite frequency content which gives a power spectral density given by (4.4) [47]. k is the Boltzmann constant. T is the temperature in Kelvin. γ is a process dependent

parameter ($\approx 2/3$). gm_i is transconductance of that stage.

$$I_{n,i}(f) = 4 * \gamma * k * T * gm_i \tag{4.4}$$

The output-referred noise power spectral density, $V_{O,n}(f)$, of the ring amplifier can be calculatd by taking the determining transfer function of each noise source to the output. The value of the power spectral density is the product of the input noise density and the square of the transfer function of the output. The power spectral densities of all the noise sources are then summed at the output as they are uncorrelated (4.5).

$$V_{O,n}(f) = I_{n,1} * (R_1 gm_2 R_2 gm_3 R_3)^2 + I_{n,2}(R_2 gm_3 R_3)^2 + I_{n,3} * R_3^2 \tag{4.5}$$

$V_{I,n}(f)$ is found by dividing the output-referred noise by square of A_{DC} (3.5). By performing this step and expanding the $I_{n,i}$ terms, the following input-referred noise equation is given (4.6).

$$V_{I,n}(f) = \frac{4\gamma kT}{gm_1} + \frac{4\gamma kT}{gm_2 * (gm_1 R_1)^2} + \frac{4\gamma kT}{gm_3 * (gm_1 R_1 gm_2 R_2)^2} \tag{4.6}$$

The result of this is not much different from a multi-stage OpAmp. The dominant noise source is the first stage. The overall power spectral noise density can be lowered by increasing the transconductance. The difference between a ring amplifier and an OpAmp is in their loop bandwidths. In an OpAmp, the bandwidth

is also determined by the first-stage transconductance. Typically the bandwidth is defined by a gm_1/C ratio where C is dependent on the OpAmp architecture. A ring amplifier's bandwidth is not defined by first stage transconductance. Its bandwidth is determined primarily by the transconductance of the last stage gm_3 (4.3). Increasing transconductance of the stages 1 and 2 while maintaining the same gain will not affect the bandwidth. Therefore, it is useful to refer to gm_i*R_i as A_i.

If we assume that the first stage noise is the dominant noise source, the integrated output-referred noise of the ring amplifier is given by calculating the integral of (4.1). The result is seen in (4.7), which can be further simplified with derived values to (4.8).

$$\overline{V}^2_{O,AMP} = \frac{\gamma * 4 * k * T}{gm_1} * \frac{G_0^2}{4\tau} \tag{4.7}$$

$$\overline{V}^2_{O,AMP} = \frac{\gamma * k * T * gm_3 * A_1 * A_2}{\beta * gm_1 * C_0} \tag{4.8}$$

In an OpAmp, this equation would have no transconductance terms in it, due to the fact that decreasing noise density by a factor X will increase the bandwidth by the same factor X. A ring amplifier has these terms decoupled. However, this small-signal estimate is limited to by the dynamic effects in the ring amplifier. As discussed earlier, the bandwidth and gain of a ring amplifier change during amplification. Given enough time, the noise of the ring amplifier will reach the value predicted by small-signal analysis. However, as a thought experiment, imagine

what might happen if the bandwidth of a ring amplifier were to go from high to effectively 0. In that way the output of the ring amplifier is acting like a sampling switch. The noise will not be predicted by small-signal analysis of the ring amplifier.

In a ring amplifier, the bandwidth will not go to zero, but it will be reduced. Only instantaneous noise at the output when it is sampled at the end of Φ_a is transferred to the next stage. It is desirable to know what the value of the noise is at a time T corresponding with the time the output is sampled. If we take the assumption that the bandwidth of the ring amplifier is higher during the beginning of amplification (that is before time T), it is reasonable to guess that the noise will likely be higher, and then reduce.

4.4.1 Transient-Noise of Ring Amplifiers

It is again difficult to calculate these exact effects of the dynamic operation. Instead, simulation tools that take into account large signal effects are used. Transient noise simulations are transient simulations with noise added. Since these same simulations capture ring amplifier settling, they are promising to use to capture noise performance. The root-mean-square output voltage can be found by running monte-carlo simulations and sampling the output voltage at a particular time.

It is important to know what the settling waveforms of the current-starved inverter ring amplifier look like in this design. First, the control voltages in Fig-

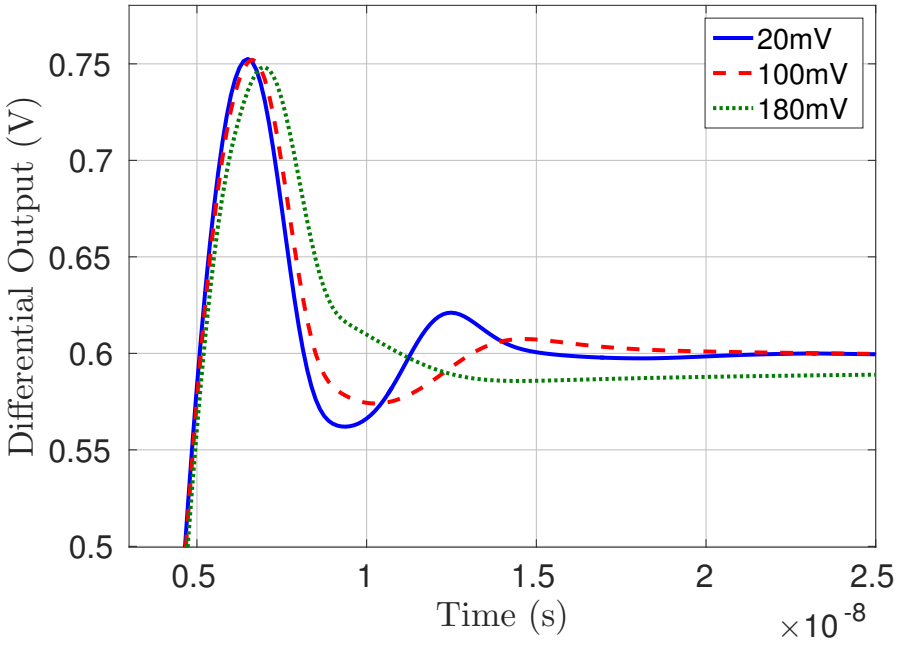


Figure 4.10: Settling response of current-starved inverter ring amplifier used in the first stage of the noise investigation pipelined ADC is shown. Three different control voltages are represented in the graph

ure 4.4 will be shown and controlled in a differential manner (V_{ctrlp}-V_{ctrln}). A larger control voltage is associated with a lower bandwidth. Three different control voltages are used, and the settling response of the ring amplifier is seen in Figure 4.10. This was simulated in a switched-capacitor amplification structure with a closed loop gain of 16. The ideal settling voltage in this case is 0.6 V. At larger control voltages the bandwidth gets too small, and the settling response of the ring amplifier is degraded.

While noise at the end of an amplification period is the critical value that will get passed on the next stage, insight can be gained by calculating the noise

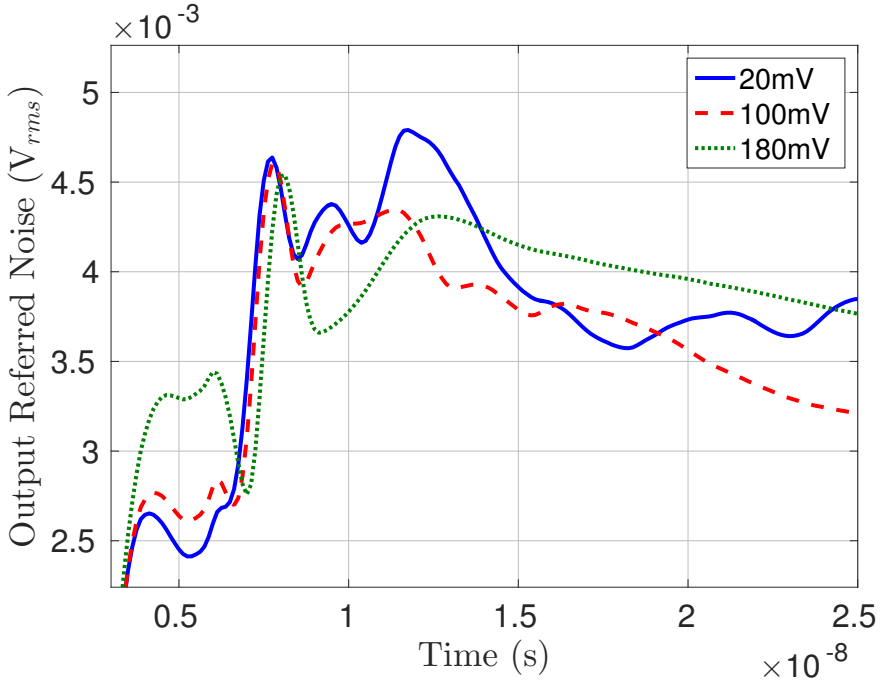


Figure 4.11: Instantaneous root-mean square output noise voltage of the current-starved inverter ring amplifier during amplification.

at different points of amplification. For the same three cases as prior, the RMS output noise during amplification is seen in Figure 4.11. As predicted, the noise performance will peak and then reduce during amplification. Of note is the case when the control voltage is set to 180 mV. If given enough time, the noise will eventually reduce below the other two control voltage settings, but the bandwidth has reduced by such a factor that noise can not be completely filtered within the amplification time (25 ns).

By knowing the output referred RMS voltage, it can be input referred and combined with other noise sources during noise budgeting of the pipelined ADC. The final settled input-referred RMS output voltage, across all reasonable control

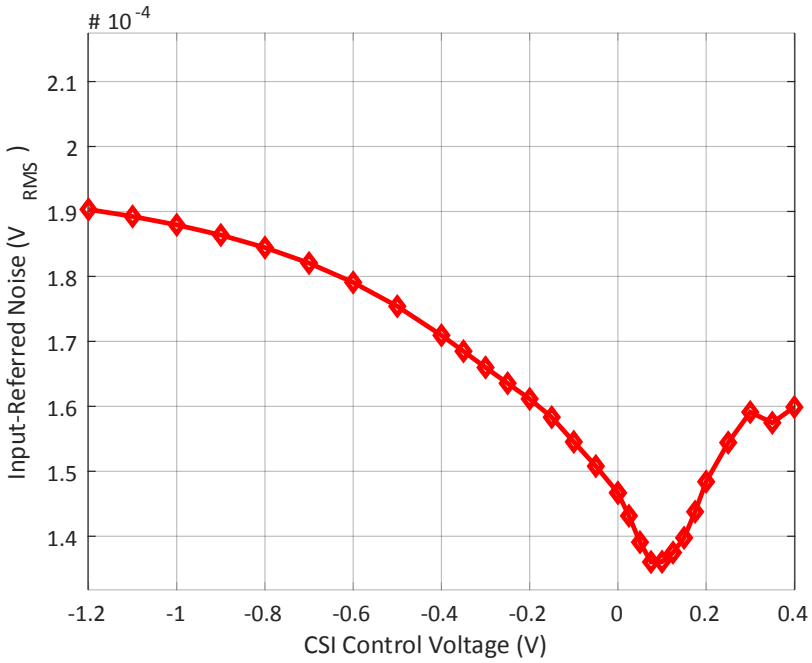


Figure 4.12: Output noise root-mean square voltage at the end of amplification for the current-starved inverter ring amplifier over a usable range of control voltages.

voltages, is shown in Figure 4.12. The assumption is made that only the ring amplifier in the first stage of the pipeline will contribute. On the left side of the graph is where the output is biased with the highest bandwidth also corresponding with the default trigger point of the current-starved inverters in the second stage. As the control voltage is increased, the bandwidth is reduced and so is the RMS noise. A local minimum is then reached where the noise begins to increase again. This corresponds with the lack of effective noise filtering discussed previously. If transient noise simulations are accurate, this should be observed in the noise floor of an ADC that uses this current-starved inverter ring amplifier. The design of a noise-investigation pipelined ADC is next.

4.5 Noise Investigation Pipelined ADC Implementation

The three key features of this prototype chip relating to the ring amplifier have been highlighted in the previous sections. They were the use of current-starved inverters to implement the deadzone and bias the output stage, the implementation of a dynamic deadzone, and an analysis of noise in ring amplifiers. These features will be incorporated into a 15b Pipelined ADC. One particular restraint on this ADC that is not common is the desire to make the ADC noise limited by the ring amplifiers acting as residue amplifiers. In this prototype ADC, this is accomplished by reducing the sampling noise compared to previous architectures [35,36]. This is necessary to validate noise simulations previously discussed. The sampling speed is 20 MSPS to provide a comparison point to other ring amplifiers designed in 180 nm CMOS.

Top-level design will be detailed explaining how ring amplifier noise is isolated by the structure. Pipeline stage design will detail timing of the pipeline-stage, MDAC circuitry, and quantizer implementation. The measurement results of this chip are detailed in Section 4.6.

4.5.1 Top-Level Pipelined ADC Design

With the goal of creating a pipelined ADC that is noise limited by the residue amplifier, it is necessary to identify other primary noise sources and mitigate their effects. In an pipelined ADC, this includes quantization and sampling noise in addition to residue amplifier noise. Quantization noise ($\overline{P}_{qe}$) is inherent to the

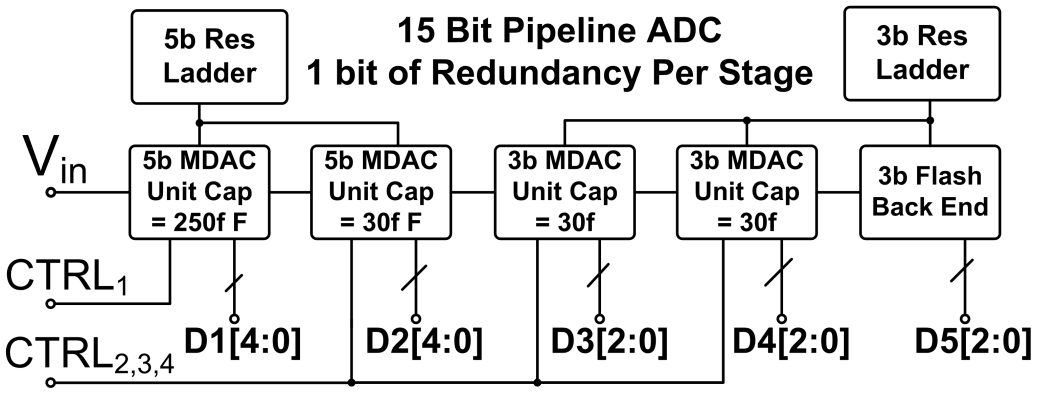


Figure 4.13: Top-level system architecture of the 15b pipelined ADC used to investigate the noise-properties of ring amplifiers.

ADC system and is reduced by increasing the resolution. Sampling noise and residue amplification are both a result of device noise whether from resistors or MOSFETs. Sampling noise ($\overline{V}^2_{samp}$) comes from the switches in sampling and is determined by a capacitance value. Residue amplifier noise comes from the active devices in the ring amplifier detailed in the previous section.

The structure of the 15b pipelined ADC is seen Figure 4.13. Each stage of the pipeline has one bit of redundancy. The first two stages have a ADC$_{sub}$ resolution of 32 level (5 bit), and the final two stages and the backend ADC$_{sub}$ are 8 levels (3 bits). The 1-bit of redundancy reduces the effective resolution of each pipeline stage by a full bit. 15b resolution is created by the digital recreation of the input signal from the pipeline stages (4+4+2+2+3 = 15). With a full-scale input signal the SQNR is 92.06 dB.

For this ADC, the full-scale single-ended reference is 1.2 V. This ADC is differential and the a full-scale input is a 2.4 V$_{pk-pk}$ signal. The integrated-noise power associated with single switch capacitor is equal to kT/C. Where k is the

Boltzmann constant, T the temperature in Kelvin, and C is the sampling capacitance. The noise in each differential channel is uncorrelated and the combined sampling noise is $\approx 2kT/C$. Each pipeline stage contributes sampling noise due its sampling capacitance. Input-referring the integrated noise power of each stage gives (4.9). Where C_i is the sampling capacitance of each stage, and G_i refers to the product of the closed-loop gain (RA_i) of the residue amplifiers prior to that stage (i.e. $G_2 = G_{CL,1}$ & $G_5 = G_{CL,1} * G_{CL,2} * G_{CL,3} * G_{CL,4}$).

$$\overline{V}^2_{samp} = 2kT * \left[\frac{1}{C_1} + \frac{1}{C_2 * G_2^2} + \frac{1}{C_3 * G_3^2} + \frac{1}{C_4 * G_4^2} + \frac{1}{C_5 * G_5^2}\right] \tag{4.9}$$

The sampling capacitance for the first stage is 8 pF (32 X 250 fF), the second stage is 960 fF (32 X 30 fF), and the third and fourth stage are 240 fF. Noise power is input referred by the squared voltage gain of the previous stage. The values of $RA_{1,2}$ are 16, while $RA_{3,4}$ are 4. Due to the high-gain of the first-stage, the sampling noise in succeeding stages is negligible overall to ADC performance. The root-mean-square voltage can be calculated by taking the square root of (4.9) which is approximately 33 μV. With the 1.2 V reference voltage, the differential LSB 14.6 μV. The full-scale SNR when just sampling noise is considered is $\approx$ 85dB.

Noise due to the residue amplifiers is analyzed by input-referring the associated noise of each amplifier. A similar result to sampling noise is observed. Due to the high gain of the first residue amplifier, the overall contribution of the following amplifiers is negligible. Taken the peak and minimum noise values from Figure 4.12,

the input referred noise of the amplifier is expected to 190 μV, at best, and 135 μV at worst when used in functional modes.

Because all these noise sources are uncorrelated, the combined noise power is found by the sum of squares of their RMS noise voltage (4.10). Peak input-referred noise is equal to ≈140 μV. Broken down into percentages of to the total noise power the amplifier noise contributes 95%, sampling noise 4.5%, and quantization noise 0.5%. This design is dominated by amplifier noise even when amplifier noise is its lowest value.

$$\overline{V}_{all}^2 = \sqrt{\overline{V}_{samp}^2 + \overline{V}_{amp}^2 + \overline{V}_{quant}^2} \tag{4.10}$$

Two resistor ladders implemented on this chip are used by the quantizers. The 5b reference ladder consumes the most power due to reference settling concerns. It is shared by the first two stage's Flash ADCs. The 5b reference ladder is shared between all backend 8 level Flash ADCs. The third stage quantizer and backend quantizer do access the 3b resistor ladder at the same time. Reference settling concerns are greatly reduced due to the lower resolution. Any reasonable glitch that may occur on the 3b reference does not affect overall performance. Power is minimal in comparison for the 3b reference ladder compared to the 5b ladder.

The analog, output buffer, and digital supply were designed for a 1.2 V. The switch supply voltage was set to 1.3 V. One current-starved inverter control signal (V_{ctrln} and V_{ctrlp}) is shared by stage 2,3,4 residue amplifier. The first stage residue amplifier has its own control signal to isolate its amplifiers noise performance. The

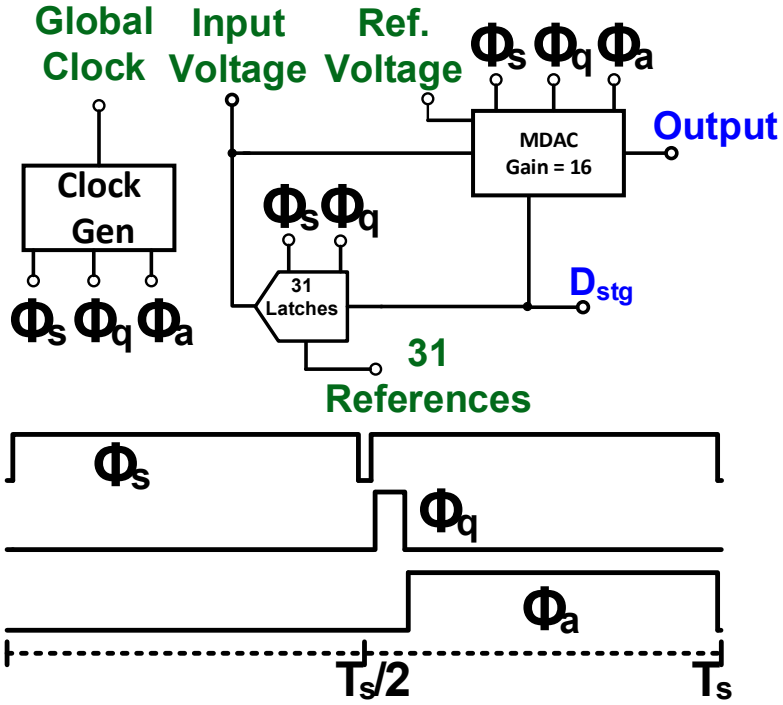


Figure 4.14: Seen is the system level diagram of the first stage of the pipelined ADC along with the timing diagram.

option for dynamic deadzone control is possible on both the first and second stage residue amplifiers.

4.5.2 Pipeline Stage Design

The design of the first pipeline stage is detailed in this section. The design of following stages is very similar except for changes in the sampling capacitance and number of levels in the ADC$_{sub}$. The pipeline-stage system diagram can be seen Figure 4.14 including a timing diagram. One half the sampling clock is dedicated to sampling (Φ_s). Following that, during Φ_q, the quantizer resolves the input-signal

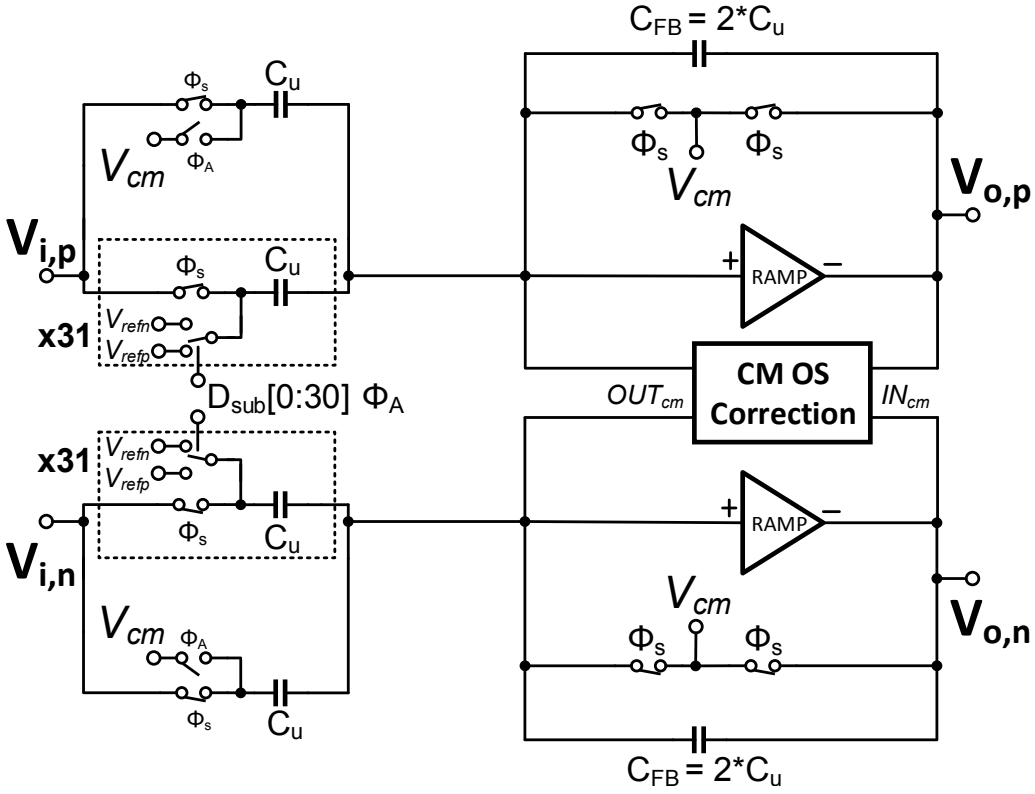


Figure 4.15: Multiplying digital-to-analog converter architecture used for residue amplification with the pseudo-differential current-starved inverter ring amplifier.

and creates D_{stg}. After that occurs the residue is amplified during Φ_A. The length of this phase is equal $T_s/2$ - T_q. T_q is the length of Φ_q and is approximately 2 ns irrespective of the sampling frequency in this design.

The MDAC with the current-starved inverter ring amplifier can be seen in Figure 4.15. The 8 pF sampling capacitance is composed of 32 unit capacitors. During amplification, the bottom-plate of 31 of those capacitors is set to either the positive reference or negative reference depending on D_{stg}. While the number of levels in this design'a ADC_{sub} could be increased to 33 and the 32^{ND} capacitor

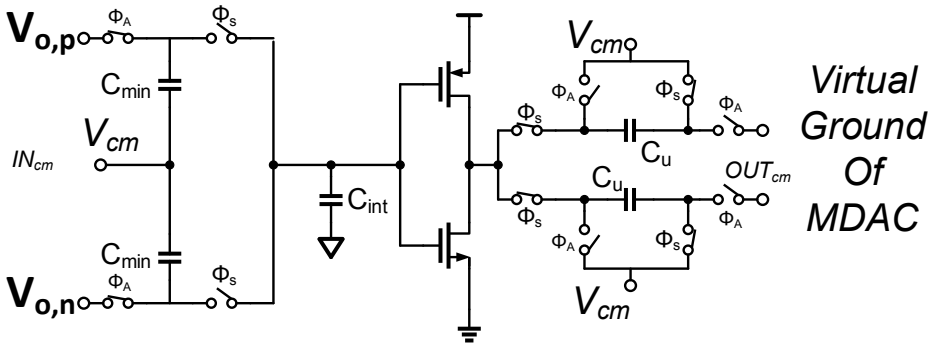


Figure 4.16: This is a circuit diagram of the circuitry used to provide common-mode offset correction at the output of the circuit in Figure 5.7.

switched to a reference voltage. Doing so would require an additional output-bit to represent all 33 levels (6 vs 5). This was avoided due to pad-frame limitations. Instead, the 32^{ND} capacitor is switched to V_{CM} during amplification.

One issue that affects differential circuit is setting the common-mode output voltage ($V_{cm,o}$). Manufacturing results such as mismatch and process result in an unpredictable ($V_{cm,o}$) . It is desirable for $V_{cm,o}$ to be approximately $V_{dd}/2$ to maximize output range of the residue amplifier. Due to the pseudo-differential nature of the ring amplifier, the difference between the common-mode of the input-signal and V_{CM} during sampling while be amplified. In a prototype chip, this can be used to control output common-mode of amplifier. However, this is less than desirable and requires a precise input common-mode. Instead, the a common-mode offset correction circuit is employed represented by CM OS Correction block in Figure 4.15.

The common-mode correction circuit can be seen in Figure 4.16. It samples the output common mode through capacitors C_min during amplification. In the

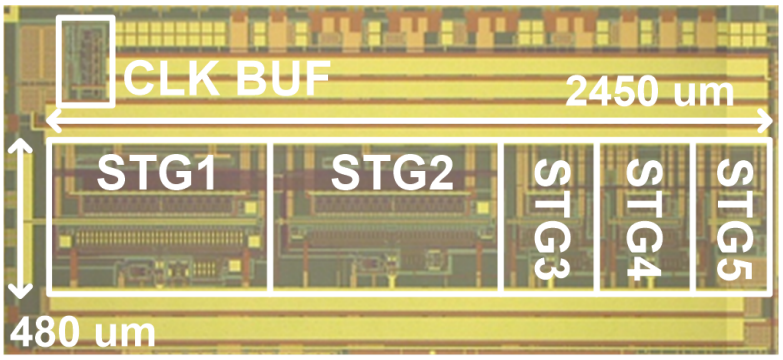


Figure 4.17: A die photo of the prototype 15b pipelined ADC with pseudo-differential current-starved inverters is presented.

sampling phase, this error is amplified and then sampled onto capacitors C_u. During amplification, this error is feedback into the virtual ground of the MDAC. This is a slow feedback loop that cannot provide instantaneous common-mode feedback during amplification. C_o is one half the value of C_u; this is done to prevent the correction circuit from degrading the feedback-factor of the MDAC significantly. However, this adds an attenuation by a factor of two in the feedback loop. The inverter provides gain to compensate. This circuit does not solve the PVT issue inherent with the common-mode level for the prototype chip but relaxes the overall accuracy requirement input common-mode aiding the testing process.

Outside of the differences between resolution and sampling capacitance in the between pipeline stages stages 2,3,4 implement a float sampling network. This prevents the propagation of a common-mode error through the stages which can saturate backend stages and degrade system level performance.

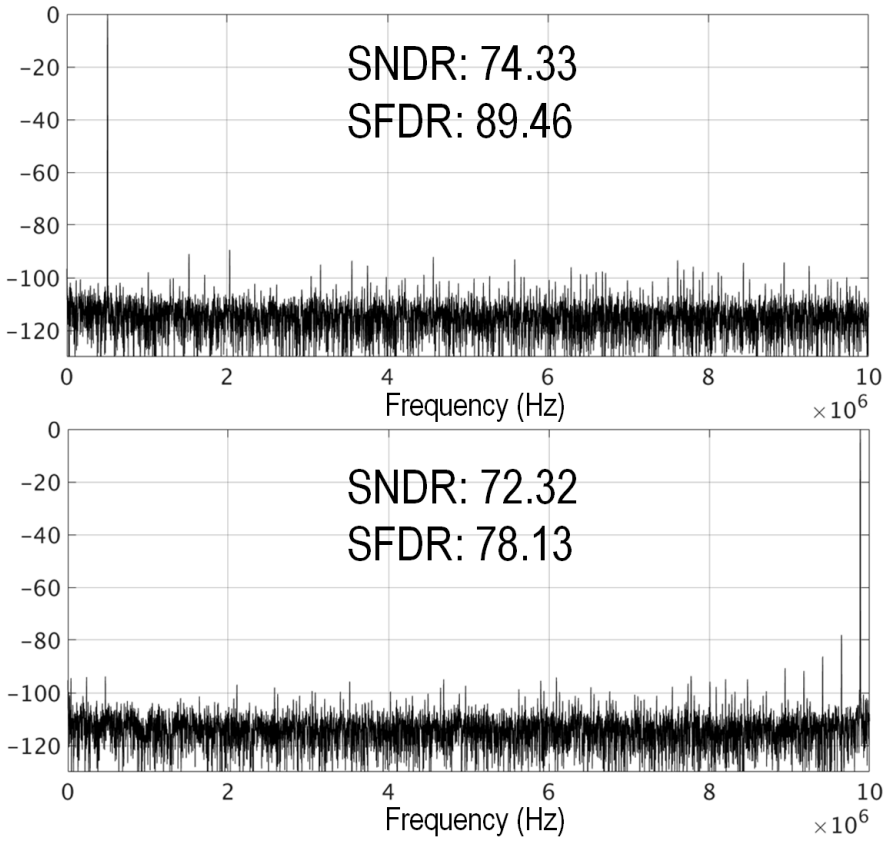


Figure 4.18: High and Low Frequency PSDs with a 10 MHz and 500 KHz input respectively with the ADC operated at 20 MSPS.

4.6 Measurements

This design was fabricated in a 180 nm CMOS process. The die photo can be seen in Figure 4.17. The overall core area is a 1.21 mm^2. Combined, the overall area of the amplifiers occupy less than 1% of the area. Overall, the ADC consumes 910 μW from a 1.2 V analog supply, 462 μW from the 1.2V reference voltage, and 1372 μW from switch, quantizer and digital supplies. Of the analog power the first stage amplifier consumes the most power at 730 μW. The digital supply was set

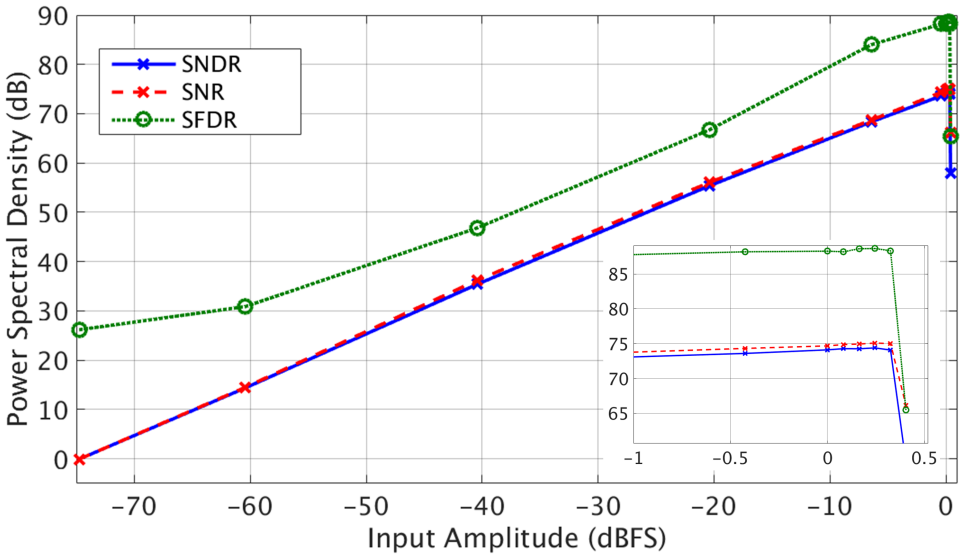


Figure 4.19: Performance measurements of the prototype ADC are plotted versus input amplitude.

to 1.25 V in measurements to account for process variations.

Power-spectral densities of the digital output are presented in Figure 4.18. A low frequency (500 KHz) and Nyquist frequency input are presented with a full-scale signal. These PSDs represent the ADC at its maximum performance. The ADC's SFDR degrades at higher input frequencies. This is caused by the amplifier performance, sampling network, and the input driving off-chip. Mismatch between ADC_{sub} path and MDAC sampling results results in an offset. This offest is amplified can eats into the redundancy range. The mismatch is largest at Nyquist frequency. The ring amplifiers in the first stage must amplify over a larger output range. However, it is still within the redundancy margin and performance is not degraded for that reason with a Nyquist Input. The main limiter is the input network and sampling interplay. Reducing series resistance of the input network

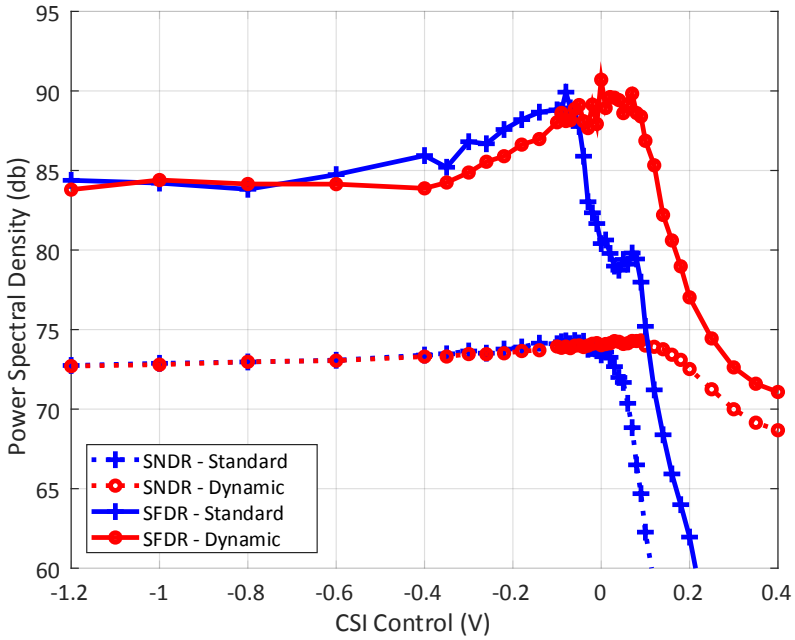


Figure 4.20: A plot of the measurement results of the pipelined ADC. SNDR and SFDR are plotted across control voltages with and without the dynamic deadzone circuity enabled.

would improve the SFDR at Nyquist frequency but would require an active input driver. This was not used in this work because the overall SNDR drop from low frequency to high frequency is <3dB given the prototype chip an effective bandwidth of 10 MHz.

Performance versus input amplitude was also measured and the result can be seen in Figure 4.19. The input frequency for this test was 500 KHz. The input amplitude can go above the full-scale reference voltage of the ADC due to the structure of the MDAC. However, eventually the output of the first-stage residue amplifier exceeds the input range of the following stages and performance rapidly drops.

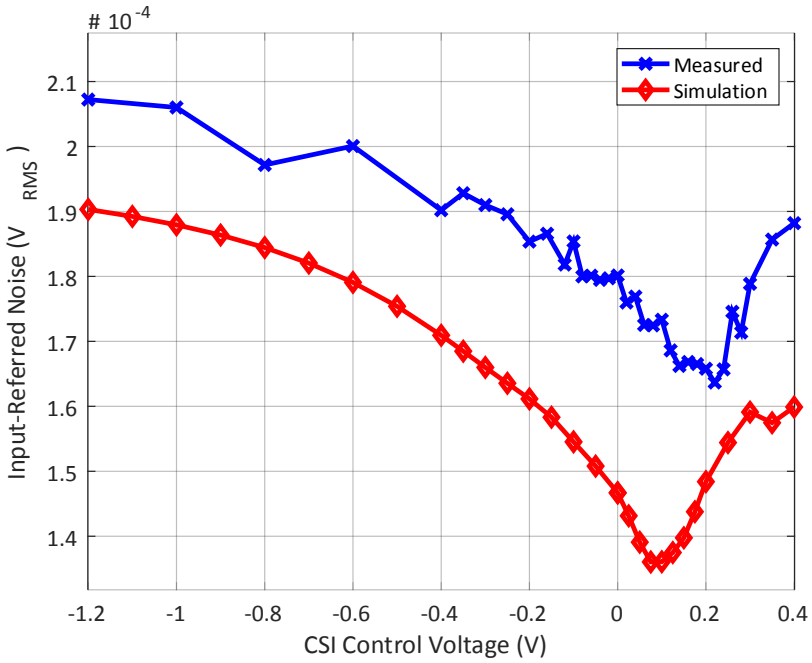


Figure 4.21: Measured and simulated noise floor of the ADC when CSI control voltage is swept.

Of particular interest is the ADC performance versus the current-starved inverter control voltages. For this, the performance is measured versus the differential control voltage (CSI Control). The differential control voltage refers to V_{dzp} - V_{dzn} in Figure 4.6. The results are shown with both the dynamic control on and off in Figure 4.20. Overall, the peak performance between the two control systems is nearly identical, but the dynamic control offers less sensitivity to the control voltage. The left of the graph corresponds with a highest bandwidth output stage, and also the nominal threshold voltage of the current-starved inverters. As CSI control is increased, the output is biased into a higher gain state. This corresponds with the improvement in SNDR and SFDR. When the control voltage becomes larger,

Technology	180 nm CMOS	
Area (mm^2)	1.21	
F_s (MHz)	20.0	
Power Amplifier (@ 1.2V) Switch (@ 1.3V) Quantizers (@ 1.2V) Digital (@ 1.25V) References (1.2V)	2.74 mW Amplifier = 910 µW, Switch = 252 µW, Quantizers = 424 µW, Digital = 696 µW, References = 462 µW	
F_{in} (MHz)	0.50	10.0
SNDR (dB)	74.33	72.32
SNR (dB)	74.89	74.21
SFDR (dB)	89.46	78.13
FoM_w (fJ/C_{step})	32.2	40.6

Figure 4.22: This is a summary of measured results of the prototype ADC with current-starved inverter.

incomplete settling of the residue amplifiers rapidly degrades performance. This ADC design was not optimized to have increased performance when using the dynamic deadzone. The peak SNDR confirms that this implementation is amplifier noise limited.

In order to confirm the transient noise simulations (Section 4.4) accurately capture ring amplifier noise performance, the noise floor of the ADC is measured. The input of the ADC is shorted, and the input-referred noise is calculated by finding the RMS value of the digital code change. The RMS value is found by multiplying that times the voltage of an LSB. The simulated and measured noise floor can be seen in Figure 4.21. As can be seen in the figure, measured and simulated values

follow the same trend. The local minimums are not aligned at the same point on the x-axis. This is attributed to process variations affecting the threshold of CSI control transistors. The difference in magnitude can be attributed to additional noise sources not accounted for, but most likely is caused by a difference in die temperature in simulation versus measurements. Overall, the accuracy of transient noise simulations is sufficient for designing ring amplifier ADCs.

A summary of the ADC performance is seen in Figure 4.22. Ultimately, the performance is limited by the settling performance of the ring amplifiers which degrade past 20 MSPS. The next chapter will describe an amplification technique that allows for high-gain and fast-settling ring amplifiers.

Chapter 5: A Dual-Path Current-Starved Inverter Ring Amplifier

This chapter details the design of a 180 nm CMOS pipelined ADC incorporating a dual-path ring amplifier in a correlated-level shifting (CLS) MDAC. The novel amplifier structure was created to address issues with high-gain ring amplifiers. Previously, it had been highlighted the a ring amplifier structure has advantages in both bandwidth and DC gain compared to an OpAmp. The benefit in bandwidth comes from the dynamic biasing that allows for improved settling time to a comparable bandwidth OpAmp. The benefit in gain comes from the cascaded nature of the ring amplifier. At least three stages of gain can be achieved while still possessing high output swing.

For high-gain applications, in small-geometries (< 65nm), the loss of intrinsic-gain in MOSFETs can leave a ring amplifier structure without sufficient DC gain. Gain can be increased in a ring amplifier structure by increasing the lengths of transistors while maintaining a similar W/L ratio. Large-signal and small-signal settling performance are both degraded by these choices. This chapter describes a prototype chip that overcomes this limitation through the use of a correlated level shifting scheme [33]. A novel ring amplifier structure is designed which reuses a first-stage differential pair for both the output paths in the CLS MDAC.

This chapter will detail the design limitations in designing high-gain ring amplifiers in Section 5.1. Correlated level shifting structures and their benefits will

be summarized in Section 5.2. Section 5.3 details the design of a dual-path ring amplifier. The architecture of a 17b Pipelined ADC used to verify this technique is presented in Section 5.4, and its measurement results in Section 5.5.

5.1 Increasing DC Gain in Ring Amplifiers

Without using calibration, high open-loop gain is needed in the residue amplifier of a pipelined ADC. The gain requirement is highest in the first stage of the pipelined ADC. As mentioned in Chapter 3, it is desirable to design a ring amplifier with the fastest transistors available in a process. From a small-signal perspective, this gives the highest frequency interior poles, and the loading of each stage by the following is minimized. This also minimizes the delay through first-two stages from a large signal perspective.

A current-starved inverter ring amplifier was designed in an 180 nm CMOS with the architecture seen in Figure 5.1. Every transistor in the main path is designed with minimum length. Settling performance of this ring amplifier can be seen in Figure 5.2(a). It is presented alongside the output settling accuracy graph in Figure 5.2(b). It is found by calculating $20 * log10(|V_o/V_g|)$. The output settling accuracy represents the open-loop settling of the amplifier. If settling is fully complete, the value given will be equivalent to the open loop gain of the amplifier. This is a useful tool for a designer as it allows visual inspection of overall settling accuracy. The peaks in settling accuracy corresponds with the zero-crossing event at the virtual ground due to ringing.

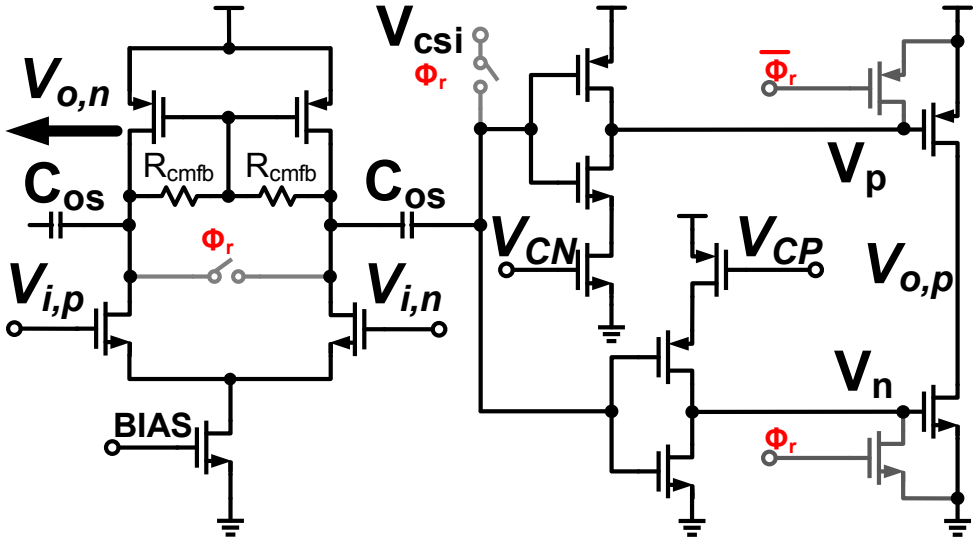


Figure 5.1: This is a circuit diagram of a current-starved inverter ring amplifier with a differential input stage.

The open loop DC gain of the minimum length ring amplifier is sufficient for 10-12 bit applications in 180 nm CMOS. In smaller geometries, the lower intrinsic gain of the MOSFETs results in a ring amplifier with even lower gain. In order to meet a higher gain requirement, the designer must modify the devices comprising the ring amplifier. This is done by increasing the length of the MOSFETs to achieve higher intrinsic gain. That can be done in the first, second or third stages. Figure 5.3 shows the result when the length of the first-stage devices has been increased. The width was also correspondingly increased to keep the drain current to W/L ratio approximately the same. It is clearly obvious that stability concerns ultimately limit the maximum possible usable lengths in a ring amplifier.

Length can also be increased in the second-stage, but it has a similar trend seen in Figure 5.3). If we apply a bit of insight gained from small-signal analysis,

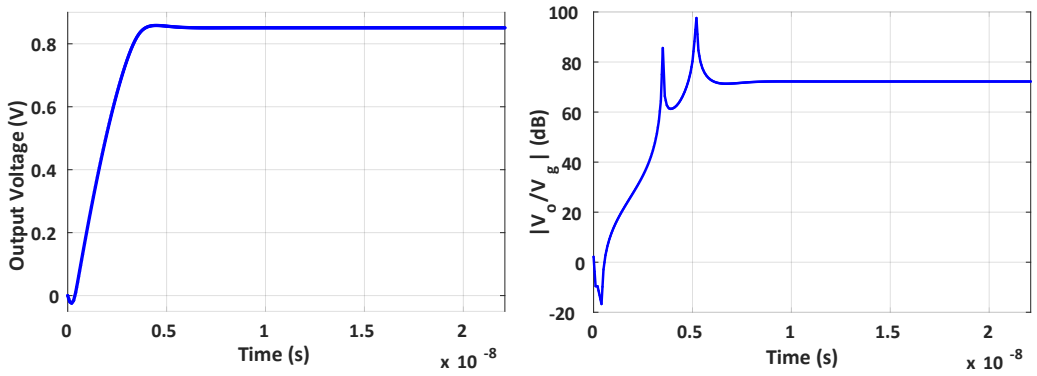


Figure 5.2: Settling performance of the current-starved inverter ring amplifier when all transistors are chosen with minimum lengths is presented.

it makes sense to increase the length of the devices in the output stage where the dominant pole occurs. Under a dominant pole assumption, increasing the output resistance will not affect stability, as the unity-gain bandwidth remains the same. Increasing the length of the output transistors not only increases their output resistance but also the intrinsic capacitors in the device. This loads the second stage.

Now the lengths of the output devices are swept, and the resulting waveforms are seen in Figure 5.4. The V_{cn} and V_{cp} are changed so that drain current to W/L ratio remains the approximately the same in all cases. The results here are more promising then increasing interior lengths. A large-signal effect can be seen that once the output devices become large enough a delay is observed before the output devices turn on and slewing starts.

Another benefit of increasing length in the output stages is that the loading effect on the second stage can be mitigated. By increasing the overall power

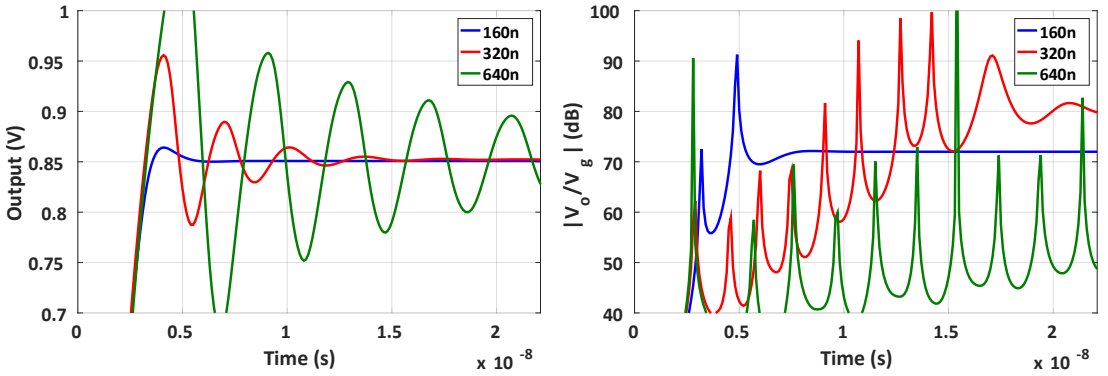


Figure 5.3: Settling performance of a current-starved inverter with first-stage lengths swept and current-density maintained is presented. Performance rapidly degrades with an increase in length.

consumption of the second stage, it is better able to drive this output stage. In the same manner as before, the output length is swept and the results are shown in Figure 5.5. The settling performance of the ring amplifier is improved at the cost of power consumption.

There is a limit to how much gain a transistor can get in a particular processes. At some point, increasing length of the transistor will have diminishing returns, and become impractically large to be realized. While in a 180 nm processes, this results in high enough DC gain expect for the extremely high resolution cases (16+ Bits). In smaller geometries, this can result in a three-stage ring amplifiers that can not achieve high enough gain for 12-bit applications. The effect of this necessitated the design of the four-stage ring amplifier [39]. An additional gain stage is added to the ring amplifier amplifier to increase the open-loop DC gain in a 40 nm processes. Another potential solution for a ring amplifier is to cascode the output stage. This comes at the cost of decreased output swing. Additionally,

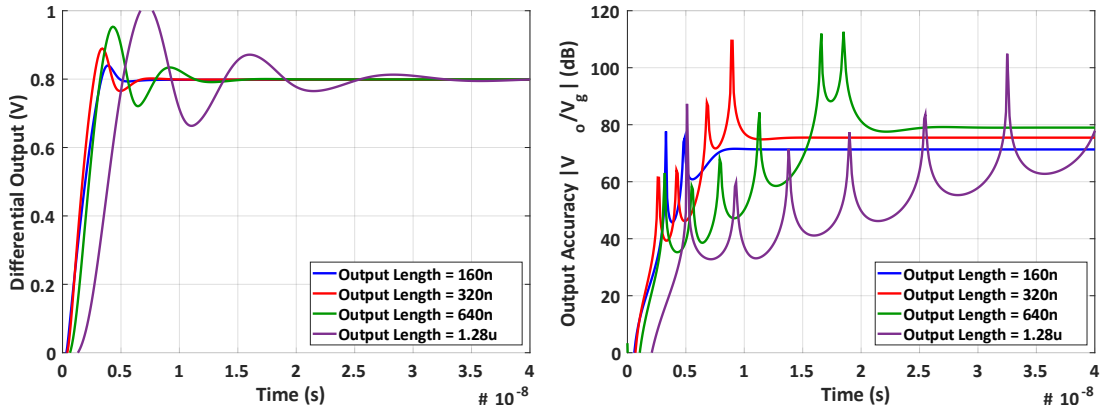


Figure 5.4: This contains the settling response of a ring amplifier when output length is swept and current-density is maintained. Loading of the second-stage by the devices in the third stage degrades performance when larger channel lengths are used.

cascoding also requires circuitry to dynamically bias the cascode stages to allow for optimal large signal operation.

From these observations, if gain isn't a requirement, the most efficient ring amplifier would use minimum length devices. It will have the smallest area, the least power, and the best settling performance. There exists a switch-capacitor technique called correlated level shifting which can be used to enhance the loop gain of an amplifier. This switched-capacitor technique will be used to make a high-gain and high-speed ring amplifier.

5.2 Correlated-Level Shifting

Correlated level shifting is a switched-capacitor technique used to increase loop-gain of a amplifier. The amplification time is broken up into distinct phases as seen

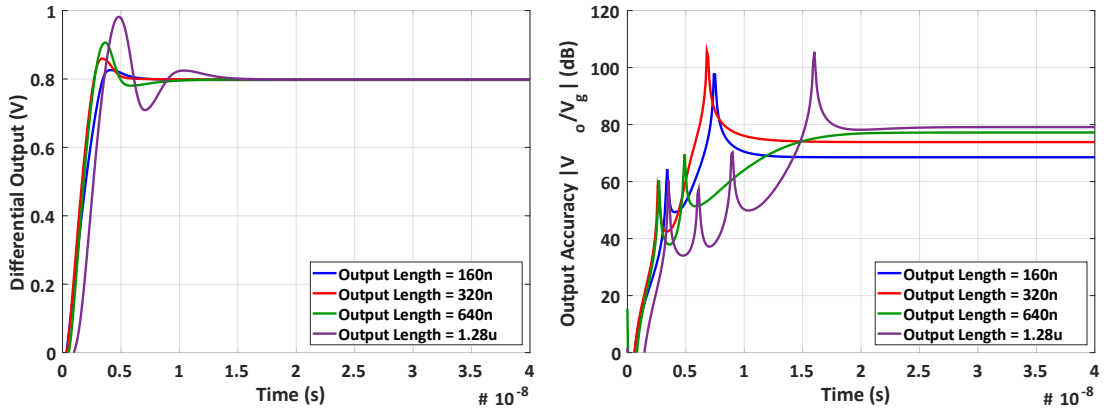


Figure 5.5: This contains the settling response of a ring amplifier when the length of output transistors is swept and current-density is maintained. The ring amplifier used in these waveforms consumes four times as much current in the second stage in Fig 5.4

in Figure 5.6. The amplification circuit is altered to include an additional capacitor (C_{CLS}) and switches. In the first amplification phase, or estimate phase (Φ_e), an incomplete settled estimate of the output voltage (V_{est}) is sampled onto C_{CLS}. In the following phase, or fine phase (Φ_f), V_{est} is put in series with the output of the amplifier. Therefore, the amplifier in the second stage is only required to settle the remaining error voltage between V_{est} and the ideal settling voltage. This effectively squares the linear loop gain of the amplifier. It also will require less output swing of the amplifier in the second amplification due to effect of the level-shifting property of C_{CLS}.

This technique was first used with a 30 dB OpAmp to achieve 60 dB performance in a Pipelined ADC [33]. Split-CLS is variation where two different amplifiers are used in the amplification. Using that technique, the amplifiers can be optimized for the separate phases. For example, the coarse phase might want a fast

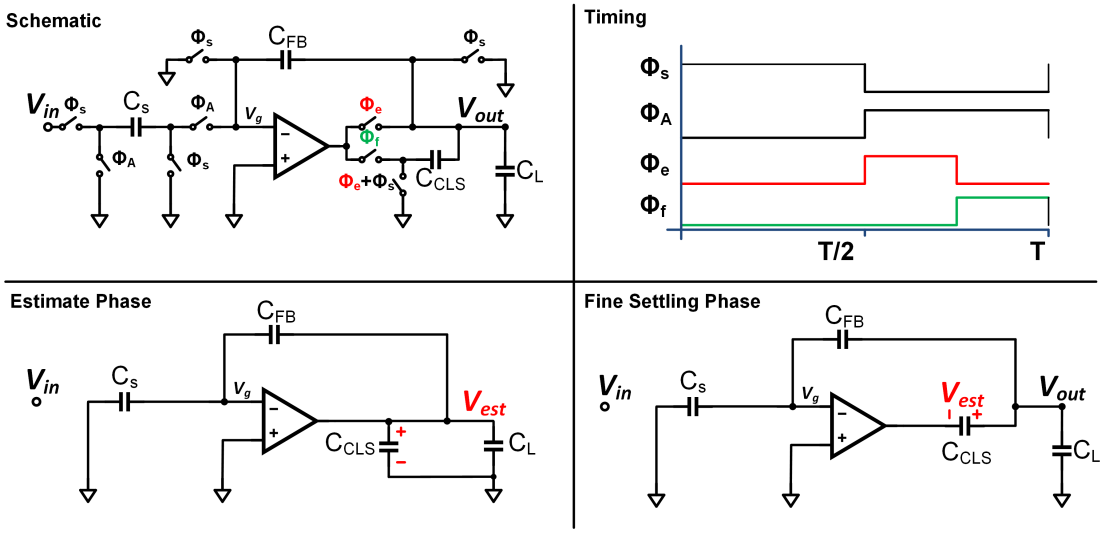


Figure 5.6: This is a diagram of a correlated level shifting amplification scheme.

high slewing stage while the fine phase might want a high-gain and low-bandwidth amplifier. This has been used with a combination of zero-crossing based charging circuit and a telescopic OpAmp [25]. The first high-precision ADC with a ring amplifier also used a split-CLS technique [34].

This prototype chip uses a partially split-CLS technique where the first-stage of a ring amplifier is reused in both phases but drives two separate output paths. A ring amplifier structure is used in both amplification phases. The design of this ring amplifier structure is covered in the next section.

5.3 Dual-Path Ring Amplifier

As previously discussed, the fastest settling ring amplifier is one with minimum length devices as they have the smallest delay and largest transition frequency

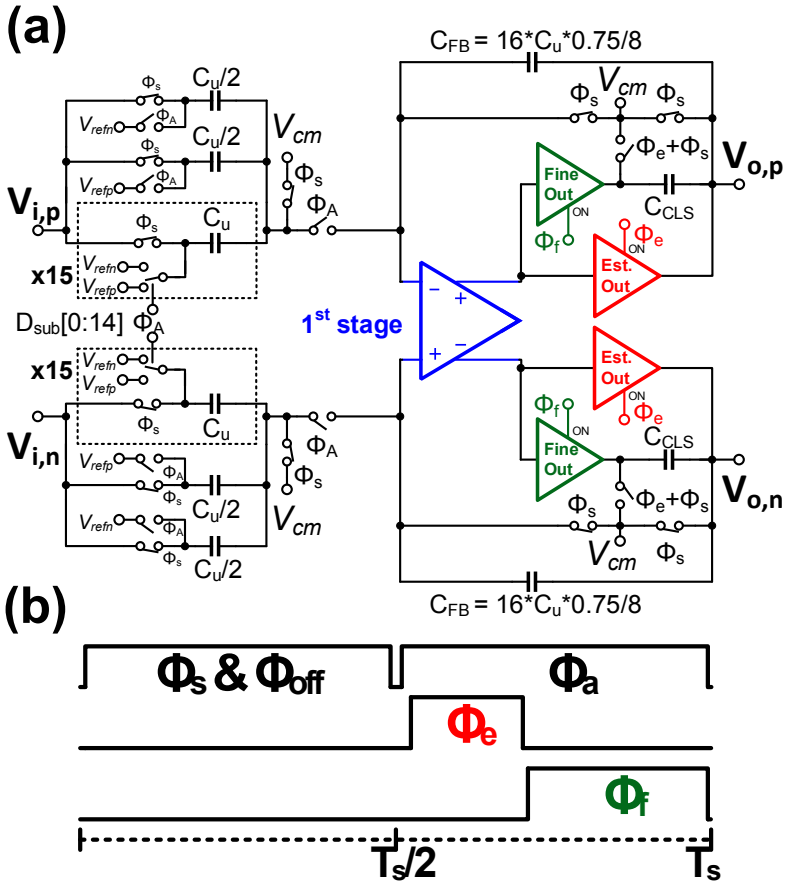


Figure 5.7: The differential multiplying digital-to-analog converter used with a dual-path ring amplifier (a). This structure provides a closed loop gain of 10 and 2/3. Timing diagram of the circuit is shown (b).

which aids in settling. The CLS MDAC structure and its timing can be seen in Figure 5.7. Similar to the previous prototype chip in Chapter 4, the front-end sampling capacitor is split up into 16 unit capacitors (C_U). 15 of those are driven by a 16 level ADC_{sub}. The relative timing of Φ_f and Φ_e is digitally controllable through a 3-bit word. The digital control aids in mitigating process variations.

The feedback capacitance is set so that the closed-loop gain is 10 2/3. There

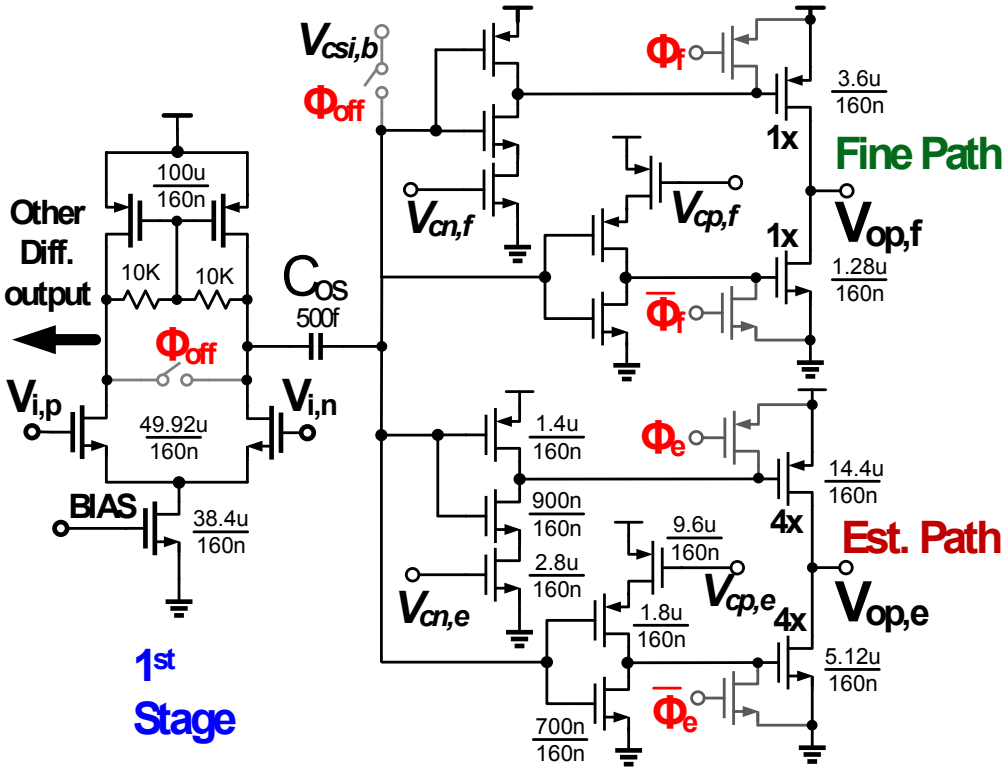


Figure 5.8: Circuit architecture and sizing of the differential dual-path current-starved inverter ring amplifier used in the first stage of the pipelined ADC. One of the differential output paths is omitted for clarity. Sizing of the second-stage is the same in both the estimate and fine output paths

is less than a full-bit of redundancy. Without any ADC$_{sub}$ errors, the ideal output range of this MDAC would be 66% of the reference voltage.

The dual-path ring amplifier used as the residue amplifier in CLS MDAC is seen in Figure 5.8. It shares the same basic architecture to the current-starved inverter ring amplifiers with a differential first stage in Figure 3.2. A second output stage has been added to the amplifier. The first stage drives both these output paths. One is used for the coarse phase of amplification and the other for the fine phase.

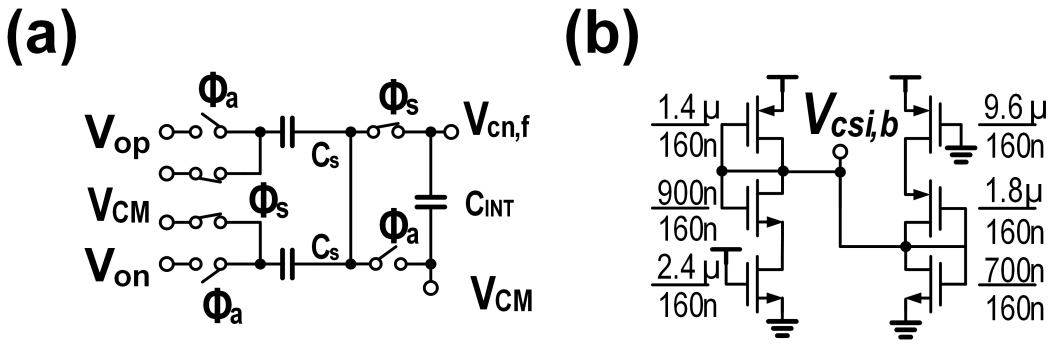


Figure 5.9: (a) Circuitry used to set the common-mode level of the output of the dual-path ring. (b) Biasing circuitry used to create the voltage $V_{csi,b}$.

Reusing the first-stage saves area and power. In both phases of amplification a wide bandwidth first stage is needed. The amplifier is designed to operated with a supply voltage of 1.3 V.

The additional output stage does add an additional capacative load to the first stage. This is counteracted by increasing the power consumption and size of the first stage. From a noise perspective, this stage is consumes a larger amount of power to reduce integrated noise at the output of the amplifier. In this design, the first stage consumes 600 uA of current. This is sufficient to make the loading effect of the extra second stage minimal. The resistors in the first-stage are part a local CMFB loop that set the output common-mode of the first stage. C_{OS} is used to level shift the output of the first-stage to the correct bias.

$V_{cp,f}$ is set off-chip to induce a low bias current in the output stage. $V_{cn,f}$ is set through a slow integration loop seen in Figure 5.9(a). It sets the bias at $V_{cp,f}$ such that the output common-mode is approximately the common-mode reference. The input bias to both the output paths is set by the replica bias circuit seen in

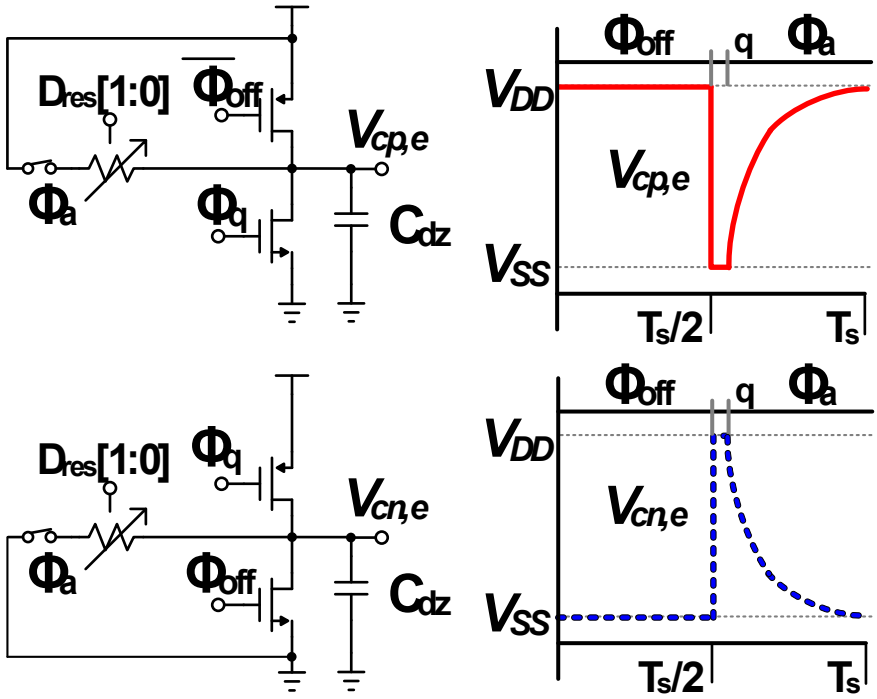


Figure 5.10: A dynamic deadzone generation circuit for the dual-path ring amplifier's estimate output path is presented.

Figure 5.9(b). The difference between the output paths is the sizing of the output stage's transistors. In the estimate path, they are four times as wide as the output path. This is because the estimate path is designed for a large slew-rate.

The estimate output path also needs to be biased through nodes $V_{cn,e}$ and $V_{cp,e}$. Instead of using an additional reference, like the fine path a dynamic deadzone is used. The dynamic deadzone is an altered from the design in [37]. Unlike that design, the desire is for the output stages static current to approach 0 instead of a small value. This is because the estimate phase does not require the amplifier to perform small-signal settling. The designed is changed to settle from either V_{dd} or V_{ss} to V_{ss} or V_{dd}, respectively, instead of a bias voltage. Figure 5.10 shows

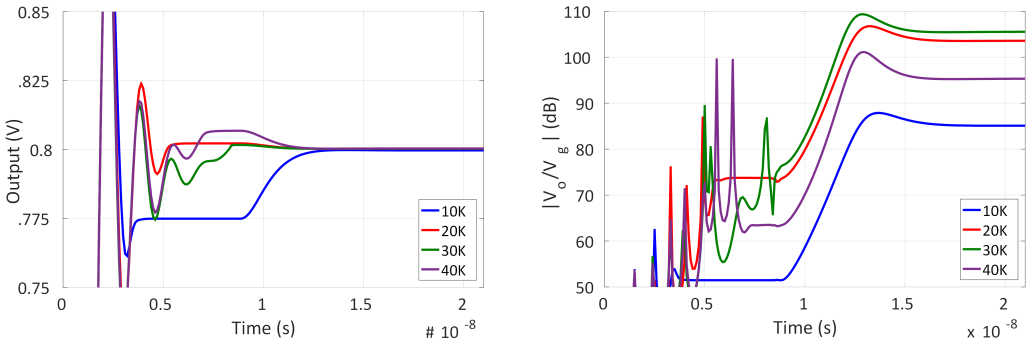


Figure 5.11: Resistor used in the dynamic deadzone biasing of the estimate path (Figure 5.10) is swept and the settling performance of the dual-path ring amplifier is observed.

the circuitry and waveforms of the dynamic bias used in this prototype chip. The resistance is digitally programmable by a 2 bit word to compensate for any PVT variations. Φ_q is the period when the input is being quantized by the ADC_{sub}.

This structure allows the sizing of the ring amplifiers output stages to be optimized for both slewing and small-signal settling. Large slew devices can degrade the small-signal settling of a ring amplifier. This is not required of the estimate path, so power can be conserved in the second stage. Undesirable incomplete settling is mitigated by the fine phase amplification. One of the benefits of using a ring amplifier is the ability to overcome a larger settling error due to the inherent dynamic bandwidth. Another benefit is that the output of the ring amplifiers is simply switched to and from a high impedance and conducting states.

The settling performance of this design is primarily controlled by three factors off chip. Two of them are set by digital registers. Those two factors are the value of the resistor in the dynamic biasing and the relative timing of Φ_e to Φ_f. The third

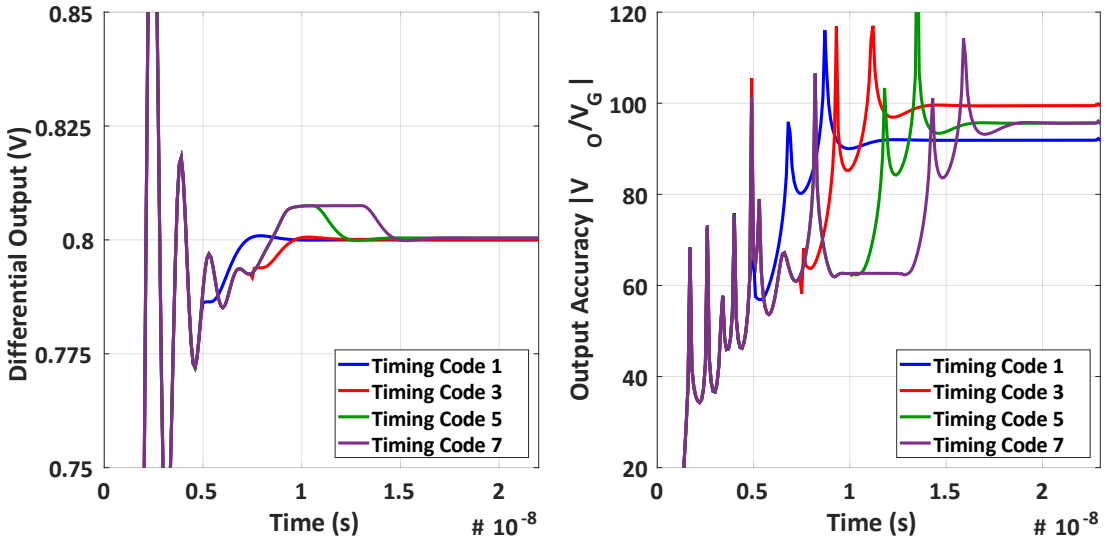


Figure 5.12: Timing of the estimate and fine amplification phases is varied and the settling performance of the dual-path ring amplifier is observed.

factor is the biasing of the fine stage. The settling performance of the dual-path CLS ring amplifier when the resistor in the dynamic bias is shown in Figure 5.11. The choice of resistance will affect how long the estimate path conducts before its current approaches 0. A larger resistance corresponds with larger conduction time of the output.

Next, the dynamic resistance is fixed to its largest value while the timing of Φ_e and Φ_f. This is seen in Figure 5.12. The timing should be managed in such a way that there is no dead time in settling response. Dead time refers to the event where the estimate path has stopped conducting, but the fine output has not been enabled.

Finally, once the resistance and timing have been optimized, the biasing of the output stage can be set. Figure 5.13 shows the settling response of the dual-path

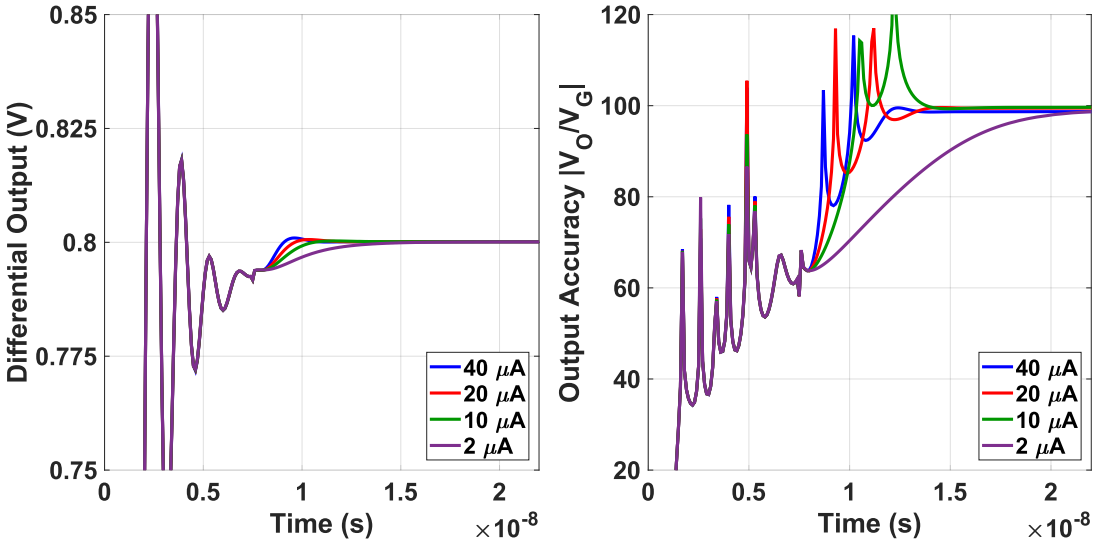


Figure 5.13: Bias current of the fine output stage is varied and the settling performance of the dual-path ring amplifier is observed.

ring amplifier when both dynamic biasing resistance and timing are fixed while the output-stage current is altered. The dynamic resistance is set to the largest value and timing code 3 is used. By optimizing these tradeoffs, high-precision amplification can occur in approximately 12 ns. In a,180 nm CMOS process at 40 MSPS, high-gain ring amplifier can be created. The design of a 17b pipeline implementing the dual-path ring amplifier is detailed in the next section.

5.4 17b Pipelined ADC

A high-resolution pipelined ADC was designed to test the effectiveness of the dual-path ring amplifier. The MDAC structure used for the residue amplifier is the same correlated level shifting scheme seen in Figure 5.7. The closed loop gain being 10 2/3 with respect to a 16 level flash-ADC results in less than one full-bit

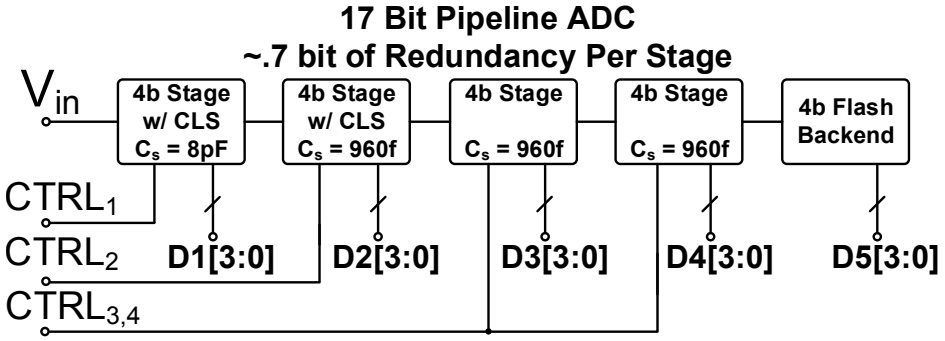


Figure 5.14: This the top level diagram of the 17b pipelined ADC implemented with the dual-path ring amplifiers in a correlated level shifting MDAC in stages 1 and 2. In stages 3 and 4 a standard differential input current-starved inverter ring amplifier in Figure 5.1.

of redundancy in this configuration. Figure 5.14 shows the overall structure of the pipelined ADC. The pipelined ADC is designed with four pipeline stages and a backend 4 bit flash ADC. Each pipeline stage approximately adds 3.3 bits to the overall resolution. This structure achieves a maximum signal-to-quantization noise ratio of 106.2 dB (17+ bits).

The high gain of the first stage helps isolate the noise performance of the system from the backend stages. The first stage total single ended sampling capacitance is 8 pF (16 pF deferentially). The sampling capacitance of the following stages is 960 fF. This ADC is designed for a 1.3 V supply voltage and a 1.2 V reference (2.4 V deferentially). The calculated ideal SNDR of this ADC in the presence of only sampling noise is $\approx$ 85 dB. This ADC was designed to operate at 40 MSPS. A block diagram of each pipeline is shown in Figure 5.15. Each stage has its own reference ladder, and clock generation circuit. The clock generation circuit is digitally controlled through a shift register. This allows the timing edges of the

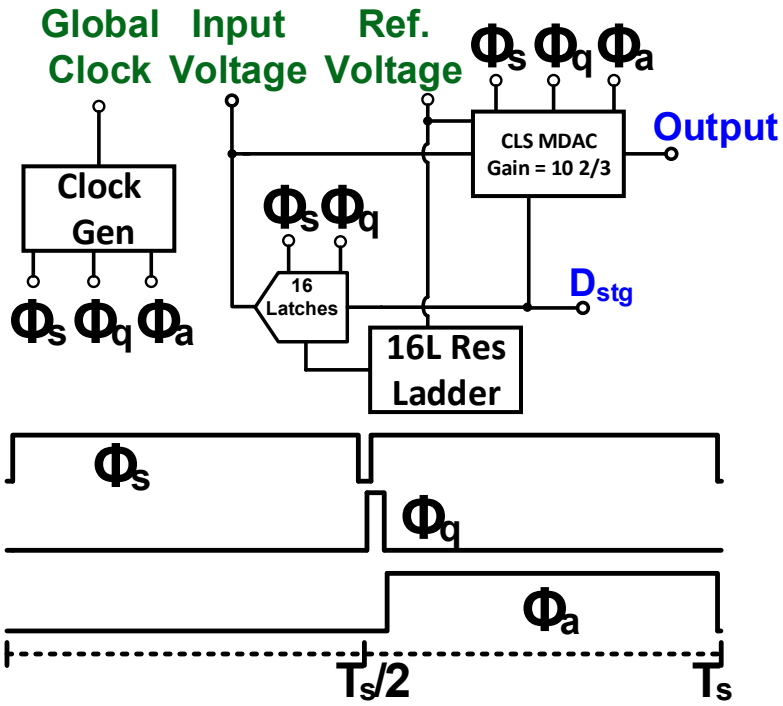


Figure 5.15: A system level and timing diagram of the pipelined stages used in the prototype 17b ADC.

CLS and quantizer clocks relative to each other to be modified after fabrication.

A one bit slice of the ADC_{sub} is seen in Figure 5.16. When the signal at the latch goes high, the comparator is resolved, and the difference between the input terminals is resolved as either a 1 or a 0. The sampling circuitry has twice as many capacitors as the previous prototype chip. Both the input and reference voltage are sampled at the same time. This allows for the resistance in the reference ladder to be chosen for primarily for power and area concerns, not settling. Before latching Φ_r occurs, after the falling edge of the sampling clock, the bottom plate of the comparators are switched to a common-mode voltage. This presents an inverted and half-scaled voltage of the difference between input and reference at

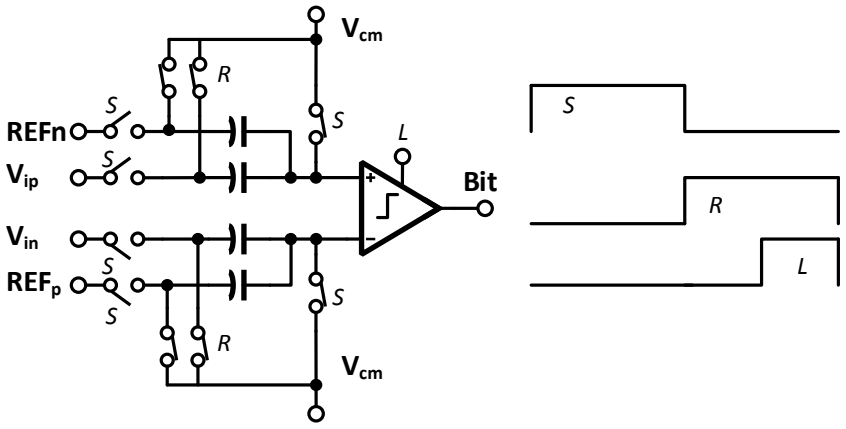


Figure 5.16: A circuit and timing diagram of a one bit slice of a 16 level flash-ADC used in the pipeline stage. In order to implement a 4b flash ADC 15 slices are used in parallel and the appropriate references are sent to each slice at nodes (REF_n & REF_pn). The 4b flash is used as the backend and ADC_{sub} of this pipelined ADC.

the differential input of the comparator. The main disadvantage of this circuit is the half-scaled input. This requires the input referred threshold of the comparators to be lower than in a two sampling capacitor structure. This is by no means a perfect quantizer structure and readers should consider alternatives.

This ADC was simulated with post layout extract parastic capacitors and transient noise enabled over a 1024 points. Simulated with analog fast spice, the lower frequency bound for the transient noise simulation is 100 hertz and the upper bound is 1 GHz. The power spectral density of the 40 MSPS FFT of the digital outputs is seen in Figure 5.17. Quantization noise, amplifier noise, and sampling noise captured in this FFT. With a full-scale input this ADC achieves 82 dB in simulation. This implies the sampling noise and amplifier noise are approximately the same. Quantization noise is at a much lower level in this simulations (106 dB level) than either sampling or amplifier noise.

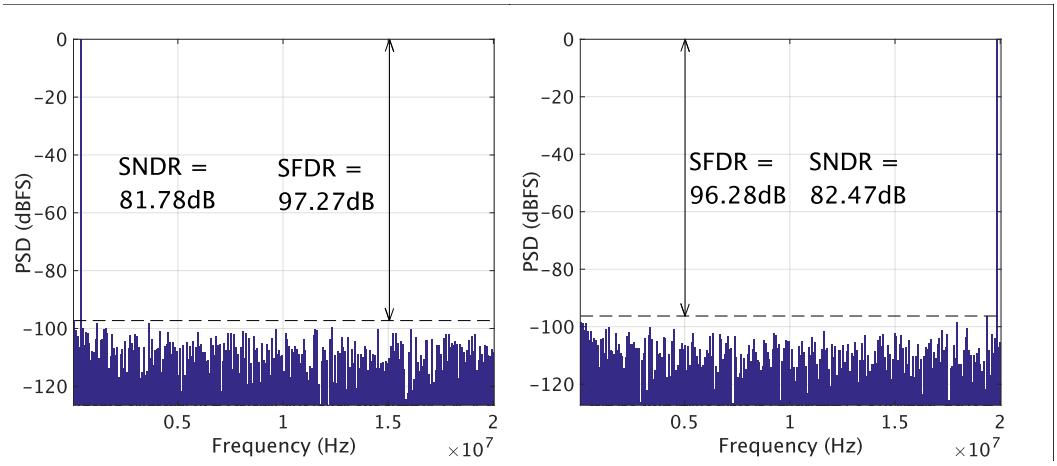


Figure 5.17: Simulated 512 point FFT power spectral density of the dual-path ring amplifier pipelined ADC with a low and high frequency input with a sampling frequency of 40 MHz.

5.5 Measurements

The die photo of this prototype chip can be seen in Figure 5.18. The total area is 2.9 mm by 0.5 mm's. Overall this ADC consume 5.78 mW of power when operated at 40 MSPS. The amplifiers consume 2.34 mW total from the analog supply. The reference power consumed by the capacative DACs is 290 μW, while the reference ladders for the ADC$_{sub}$ consume 280 μW. The quantizers in the ADC$_{sub}$ consume 1.03 mW. The switch supply consumes XY watts. The digital circuitry uses XYZ watts.

Testing is still ongoing on this chip. 17 KHz input frequency Full-Scale power spectral densities of the ADC operating at 20 MSPS and 40 MSPS can be seen in Figures 5.19(a),(b) respectively. The 20 MSPS PSD is presented as a contrast to the 40 MSPS version. The increase in amplification time provides a contrast of

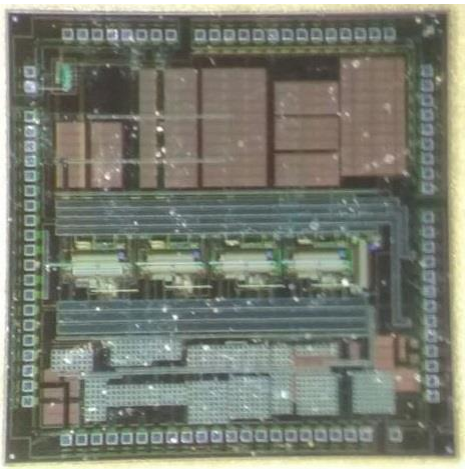


Figure 5.18: This is a die photo of the prototype ADC fabricated in a 180 nm CMOS process.

an amplifier fully-settled (20 MSPS) and one still nearly finished (40 MSPS). No calibration is applied to these results. The linearity in both cases remains high (88+ dB SFDR). This technique can be used to settle high-gain ring amplifiers quickly.

The least promising result is the lower than desired overall SNDR. This is due to an increased noise floor. The exact cause of this is still being investigated in the lab. Potential causes include unaccounted for high frequency noise associated with the estimate path output. During slewing, very high bandwidth is exhibited by the amplifier. It is under consideration that the model in this process may not accurately account for that high frequency information. A possible explanation for why that did not affect previous chips is due to the rapid turn-off associated with the dynamic biasing. Prior implementations could filter the noise towards the end of amplification while the estimate path can not as it is turned off before then.

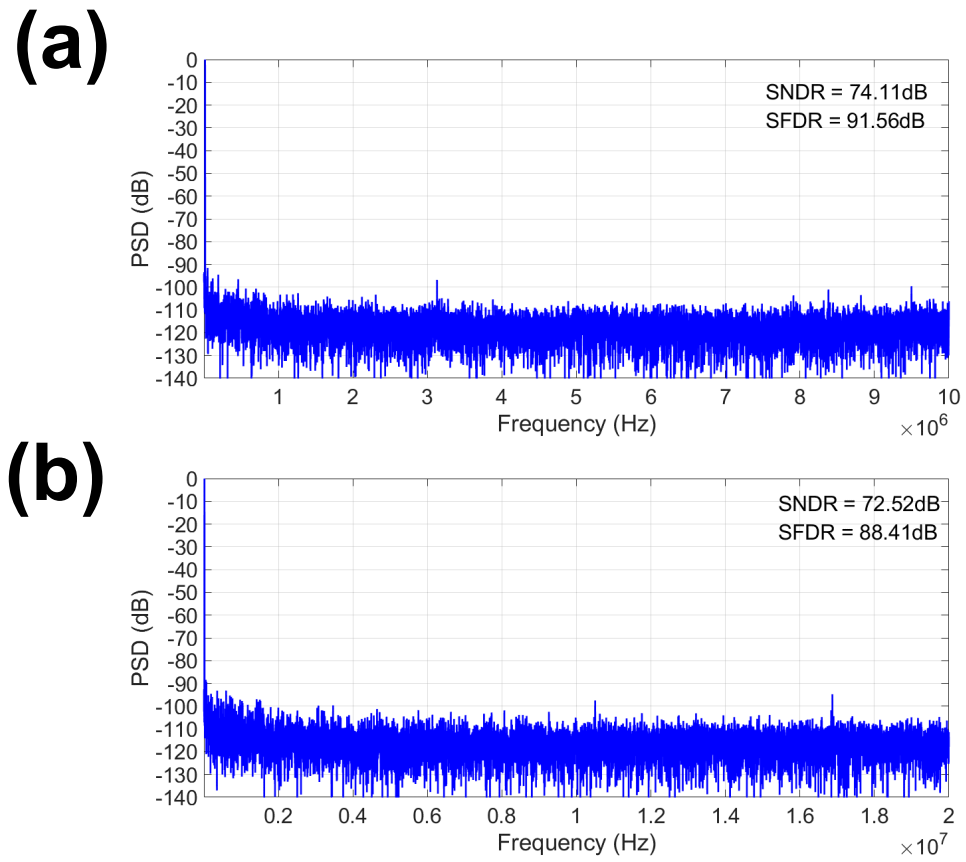


Figure 5.19: This is the measured 2^{15} point FFT PSD of the prototype ADC operated at 20 MSPS (a) and 40 MSPS (b) both with a full-scale 17 KHz input.

Chapter 6: Conclusion

This dissertation covered the topic of ring amplifiers for switched-capacitor circuits. Two pipelined ADCs using ring amplifiers are detailed. The operation of ring amplifiers was first covered. The three-stage cascaded structure of ring amplifiers inherently provides high open-loop gain. Ring amplifiers function well as residue amplifiers with high open-loop gain requirements. Ring amplifiers are inherently efficient at driving switched-capacitor circuits because they posses dynamic biasing.

Dynamic biasing allows ring amplifiers to outperform the response predicted by small-signal analysis. In the early moments of amplification, a ring amplifier possesses increased bandwidth and slew capability. This results in a large portion of settling completed very quickly. The ring amplifier will return to its small-signal bias. The remaining portion of settling then occurs with lowered bandwidth. This allows ring amplifiers to be designed with lower bandwidth than a comparable OpAmp. Lowering the bandwidth reduces integrated noise performance and saves power.

The dynamic bandwidth of the ring amplifier also affects the performance trend when feedback-factor or closed-loop gain of the switched-capacitor circuit is altered. Compared to an OpAmp, a ring amplifier becomes increasingly more efficient in lower feedback factors. This effect occurs because the dynamic slewing is signal-independent, and its effect remains constant when the feedback factor is altered.

Due to this factor ADC design space is opened up. High closed-loop gain residue amplifiers can be added to system level design of ADCs. In particular ring amplifiers enable they use of pipelined SAR ADCs.

This dissertation detailed the design of a current-starved inverter ring amplifier. Current-starved inverters are used to replace the capacitors and inverters of the second stage of a ring amplifier. By adjusting the control node of the current-starved inverters, the output stage of the ring amplifiers is biased and a deadzone is created. A prototype chip was fabricated to demonstrate the performance of current-starved inverter ring amplifiers. The prototype chip also demonstrated a dynamic deadzone bias for the current-starved inverter ring amplifiers. This prototype ADC was also used to evaluate the accuracy of transient noise simulations of ring amplifiers.

Current-starved inverter ring amplifiers were expanded on in a second pipelined ADC. The observation was made that low gain ring amplifiers have the best settling performance. A dual-path current-starved inverter ring amplifier was developed for high accuracy and speed settling performance. This new design required the use of a correlated level shifting amplification circuit. With this technique ring amplifier speed can be increased. This enabled the pipelined ADC to increase from 20 MSPS to 40 MSPS in a 180 nm CMOS process. A prototype chip was fabricated and measured to demonstrate this technique

6.1 Ring Amplifier Future Work

Ring amplifiers appear to be a promising circuit for future switched-capacitor circuits. This does not mean that there is no progress to made in their design. This section will briefly cover some areas where ring amplifiers can be improved.

One of those is the dual-path ring amplifier. Measurement results do still not match simulation, and those are an avenue to explore. Outside of exploring the mismatch between simulations and measurements, other features can be improved. One of those is the timing of coarse and fine phases of amplification. In the current implementation, it is handled by delay lines. Because of the dynamic deadzone, the estimate output phase will enter an off or non-conducting state. If that condition can be detected, and used to turn on the fine phase performance can be optimized. Power is also reduced due the elimination of the delay line.

Another large concern for ring amplifiers is performance in the face of PVT variations. These variations can cause ring amplifiers to have an unstable settle response. Ring amplifiers are particularly vulnerable to these effects as many of their small-signal parameters are influenced by these variations. The output stage is the most important to keep stabilized across corners. Replica biasing can be approached, but the output stage is small. One possible result is that replica biasing is limited due to mismatch. Techniques such as floating current source biasing which uses the actual output stage are promising. Another possible avenue is to borrow master-slave techniques from filter design. A ring amplifier is just a stabilized oscillator, after all.

Another avenue for ring amplifier design is increasing the application space. Ring amplifiers have been used as residue amplifiers. Nothing inherently stops them from being used in a switched-capacitor integrator. Where they really can be expanded is into non switched-capacitor circuits. Low-dropout regulators are one such field. The large capacitance at the gate of the dropout transistor can be driven by a ring amplifier.

To future students and researchers, ring amplifiers only require a bit of creativity and a few iterations of simulations to appreciate. Work is always the most impactful when it breaks design trends and tradeoffs that already exist. One way to gain an appreciation of these tradeoffs is to just start designing. Sometimes the hardest part is just getting into the pool.

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