Highly Linear Noise-Shaped Pipelined ADC Utilizing a Relaxed Accuracy Front-End

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Abstract

A noise-shaped pipelined ADC is presented in this paper. A minimal complexity $\Delta\Sigma$ modulator in the first two sub-ADCs and residue feedback in the latter stages lead to high-order noise shaping. This also leads to reduced sensitivity to analog imperfections in the front-end stage. Implemented in 0.18μm CMOS, the ADC achieves 12 ENOB with 64 MHz clock at 6X OSR while using only a 9-bit linear front-end multiplying-DAC (MDAC). The delta-sigma sub-ADCs dissipate 400μW extra power (out of 13.9mW total power) while significantly enhancing the the overall ADC linearity.

Index Terms

$\Delta\Sigma$ modulation, pipelined analog-to-digital converters, oversampling converters, noise shaping, switched-capacitor circuits, loop filter, feedback DAC.

I. Introduction

Oversampling ADCs are widely used in high accuracy wired and wireless communication applications. Recent advances in the communication systems have lead to the demand for increased signal bandwidth in oversampling ADCs. The signal bandwidth (BW) of oversampling ADCs can be increased either by increasing the sampling rate or reducing the oversampling ratio. Sampling speed is usually limited by the technology, and aiming for higher sampling rate results in higher power dissipation. A more practical approach to increasing the signal BW is to reduce the oversampling ratio (OSR). An important challenge in the design of low OSR ADCs is maintaining the accuracy at low OSRs, since reduced OSR means increased in-band quantization noise. All low OSR ADCs will require higher order noise shaping and more

number of quantization level to suppress the in-band quantization noise sufficiently. However, the high order noise shaping and aggressive quantization will result in increased design complexity, working against the power/area efficiency goal.

Several techniques have been reported to improve the accuracy of oversampling ADCs at low OSRs. One is to use a cascaded architecture [1]- [5]. In a cascaded ADC, the quantization error of each stage is processed by the following stage. The output of the stages are combined to cancel the quantization errors of all stages preceding the last stage. Such cascading is common to many types of ADCs, including pipelined ADCs [6]- [8] and MASH $\Delta\Sigma$ modulators [1]- [26]. The MASH converters use a cascade of $\Delta\Sigma$ modulator loops to increase the order of the noise shaping and allow low OSR operation with minimal design complexity. However, such cascaded architectures suffer from the quantization noise leakage of the first stage and requires highly accurate circuit components [18].

The pipelined ADC, a member of cascaded architectures, can provide a power efficient method for aggressive quantization of input signal and can be used as a standalone oversampled ADC. However, the accuracy of the standalone oversampled pipelined ADC is limited by the nonlinearity of the front-end stage and the quantization noise of the backend stage. Reported standalone oversampled pipelined ADCs [10]- [11] only provide a solution to improve the capacitor ratio mismatch and dissipate a significant amount of power to achieve the desired accuracy at low OSRs.

Recently, a hybrid combination of $\Delta\Sigma$ and Pipelined ADCs was introduced by the authors [12]- [15] as an improved option to cascaded modulators. This architecture employed a full pipelined ADC as the quantizer of a single-loop $\Delta\Sigma$ modulator and used the latency of the pipelined ADC to improve the noise shaping. Hence, it provided aggressive quantization and noise shaping that is required for low OSR applications. Moreover, the Hybrid $\Delta\Sigma$/Pipelined (HDSP) architecture is inherently a single-loop architecture, and thus it has relaxed design requirements unlike the MASH counterpart.

In this paper, a new and more efficient hybrid combination of $\Delta\Sigma$ and pipelined ADCs is introduced, where a $\Delta\Sigma$ ADC is used to aid the linearity of an oversampled pipelined ADC. An important goal behind this approach is to reduce the overhead of $\Delta\Sigma$ in the overall power/area consumption of the hybrid combination without degrading the overall accuracy. In this work, noise shaping is exploited both in the front-end as well as the back-end stages of a pipelined

ADC. A new pipelined front-end stage is introduced, which uses a coarse $\Delta\Sigma$ modulator as its sub-ADC. As a result, a shaped quantization noise is processed by the front-end stage, resulting in suppression of MDAC analog imperfections (including opamp gain error, capacitor mismatch and incomplete settling). The Noise-Shaped Two-Step (NSTS: section IV-D) ADC is used as the back-end stage to further suppress and shape the final quantization noise power.

In short, the proposed architecture is exactly the opposite of the HDSP [15]. In the HDSP architecture, a pipelined ADC is used to enhance the noise shaping and quantization of a delta-sigma ADC, while in this proposed architecture a delta-sigma sub-ADC is used to improve the linearity of a pipelined ADC. The delta-sigma sub-ADC uses only an insignificant portion of in the overall power and die area since it is used only for the purpose of coarse quantization of input signal. Furthermore, the proposed combination self-contained with local feedback paths in each stage, and this reduces design and layout complexity compared to the HDSP [15].

The prototype ADC was fabricated in a 0.18μm CMOS technology. The measurement results demonstrate a 15dB linearity improvement (resulting from using the proposed technique) with only 400μW (less than 5 percent of the total) consumed in the $\Delta\Sigma$ sub-ADCs.

The details of the architecture and the implementations is presented in this paper as follows: In section II, the noise-shaped pipeline stage (NSS) is introduced. The proposed noise-shaped pipelined ADC details are presented in section III. In section IV, the circuit realization details are provided. The measurement results and conclusions are given in section V.

II. Noise-Shaped Stage (NSS)

In pipelined ADCs, errors from the front-end stage usually limit the overall accuracy of the ADC. The noise shaping properties of a $\Delta\Sigma$ can be used to mitigate this imperfections of the pipeline front-end stage. Descriptions of such improvement is given in this section.

A. Noise-shaped stage (NSS) architecture

Shown in Fig. 1(a) is a typical first stage of a conventional pipelined ADC. In this conventional architecture, the sub-ADC quantizes the input voltage, and the DAC converts the digital code to an analog signal. The residue (quantization noise) is extracted and multiplied by the inter-stage gain (G). In this stage, any error in the residue amplifier directly distorts the output residue.

The proposed noise-shaped stage (NSS) is shown in Fig. 1(b). The sub-ADC is a coarse (i.e. minimal complexity) $\Delta\Sigma$ ADC. The output code is applied to a filter H_F and converted to an analog signal via the DAC. The input signal is also filtered for equivalent matching of signal paths (differences/mismatch tolerated due to built-in redundancy in a pipelined ADC). The residue is amplified by G.

The output residue of the NSS includes high- and low-pass shaped quantization noise. The low-pass filtering (H_F) does not affect the signal band. As a result of $\Delta\Sigma$ modulation, the in-band quantization noise is shaped and more randomized. Thus, the overall inaccuracies in the signal band, resulting from gain error and nonlinearity, is suppressed. This includes errors due to finite opamp gain, nonlinearity in the residue amplification, capacitor mismatch, and incomplete settling. Therefore, a residue amplifier with lower accuracy may be employed for higher precision oversampled pipelined ADC.

Because the high-pass noise transfer function (NTF) of the $\Delta\Sigma$ modulator amplifies the out-of-band quantization noise, a low-pass filter H_F is needed to reduce the out-of-band quantization noise and prevent overloading in the amplifier (G). The low-pass filter is also used in the signal path so that the input signal is processed similarly in both paths. Any remaining mismatch of the two paths results in a small leakage which does not affect the overall accuracy due to the built-in digital redundancy in the pipelined ADC. Because the $\Delta\Sigma$ modulator in the NSS is used only in the coarse sub-ADC quantization of the input signal, it may be inaccurate and consume very little power.

B. Error suppression in NSS

As mentioned earlier, the main feature of the NSS is the reduced sensitivity to analog imperfections. This includes sensitivity to any error which changes the inter-stage gain from its nominal value.

The output signal of NSS is a shaped quantization noise and can be expressed as

$$V_r = -H_F \cdot NTF \cdot G \cdot Q \tag{1}$$

In (1), H_F, NTF, G and Q denote the frequency response of the low-pass filter, the noise transfer function of the $\Delta\Sigma$ modulator, inter-stage gain and the quantization noise, respectively.

The NTF is usually in the form of $(1-z^{-1})^N$ where N is the order of $\Delta\Sigma$ and it will be shown later that H_F may be in the form of $\frac{(1+z^{-1})^N}{2^N}$ for a proper operation of the NSS MDAC. Hence, V_r may be expressed as

$$V_r = -\frac{(1-z^{-2})^N}{2^N} \cdot G \cdot Q \tag{2}$$

The transfer function in (2) has N zeros at DC, and N zeros at $\frac{f_s}{2}$. Hence, both in-band and out-of-band quantization noise are shaped at the output. MDAC analog imperfections make the inter-stage G inaccurate. Ideal inter-stage gain (G_{ideal}) is $\frac{C_S}{C_F}$ (given ideal capacitor values) which is the ratio of the sampling over the feedback capacitor. At the presence of analog imperfections, such as the capacitor mismatch, opamp gain error and incomplete settling, G can be expressed as

$$G = -\frac{C_S + \Delta C}{C_F}\frac{\beta A_{DC}}{1+\beta A_{DC}}(1-e^{-\frac{t}{\tau}}) \tag{3}$$

$$\Delta G = G - G_{ideal} = \frac{\Delta C}{C_F}\frac{\beta A_{DC}}{1+\beta A_{DC}}(1-e^{-\frac{t}{\tau}}) - \frac{C_s}{C_F}\frac{1}{1+\beta A_{DC}} - \frac{C_s}{C_F}\frac{\beta A_{DC}}{1+\beta A_{DC}}e^{-\frac{t}{\tau}} \tag{4}$$

here, C_S and C_F are the sampling and feedback capacitors; β is the feedback factor; A_{DC} is the dc gain of the amplifier; τ is the time constant of the amplifier settling; t is the half-sampling period ($\frac{T_s}{2}$) and ΔG is the inter-stage gain error. Mismatch between capacitors (C_F and C_S), the finite DC gain of the opamp and settling error make the inter-stage gain inaccurate and causes static or dynamic settling error. In the proposed architecture, the shaped quantization noise is processed by the MDAC and the inter-stage gain error appears at the output as follows

$$\Delta V_r = \frac{(1-z^{-2})^N}{2^N} \cdot \Delta G \cdot Q \tag{5}$$

Hence, the linear in-band and out-of-band inter-stage error is shaped similar to the quantization noise. Matlab simulation results show that the second order NSS is 14dB and 25dB (at 4X and 8X OSR, respectively) more linear compared to the conventional MDAC.

Any nonlinear inter-stage gain error is also suppressed in the proposed scheme. The rms power of the MDAC output signal (V_r) is significantly reduced compared to the traditional pipeline MDAC. Hence, its respective nonlinear distortion power is attenuated as well. Note that this property holds because both the in-band and the out-of-band quantizations are shaped. Shaping just the in-band quantization (i.e. using a $\Delta\Sigma$ sub-ADC without a low-pass filter) would significantly increases the out-of-band rms quantization power and consequently the overall

nonlinear distortion power (though the SFDR would still improve). Simulation results show that the first order in-band and out-of-band noise shaping (resulting in $\frac{1-z^{-2}}{2}$ combined with low-pass filtering) reduces the overall rms quantization power by a factor of 1.7, while just first order in-band noise shaping ($1 - z^{-1}$) increases the rms quantization noise power by a factor of 2. This can be inferred also from the voltage swing and output spectrum of the MDAC as shown in Fig. 2.

To demonstrate the effectiveness of the proposed NSS, Matlab simulations have been performed on the proposed NSS and the conventional pipeline input stage. The sub-ADC used in these stages resolves 3.5 bits and G is 8. One bit redundancy is considered between the pipelined stages. In both cases, the input stage is followed by an ideal back-end ADC, to study only the front-end effects. The residue amplifier was assigned a nonlinear DC gain, such that effective loop gain changes from $40dB$ to $25dB$ when its input voltage swings from $0.6V_{omax}$ to V_{omax} , and from $-0.6V_{omax}$ to $-V_{omax}$. This is equivalent of 1-4 percent non-linear variation in G. For input voltages between $-0.6V_{omax}$ and $+0.6V_{omax}$, the effective loop gain is $40dB$. The output spectra of the ADC are shown in Fig. 3 for the NSS with first- and second-order noise shaping, and for the conventional stage. Clearly, harmonics caused by the nonlinear opamp gain are effectively suppressed in the NSS, even at low OSRs. At an OSR of only 4, and with nonlinear opamp gain, the SNDR is $73dB$ for the first-order NSS, and $80dB$ for the second-order one. The conventional stage gives only $62dB$. At $OSR = 8$, the $SNDR$ is $78dB$ and $91dB$ for the first-order and the second-order NSS, respectively, while for the conventional stage $SNDR = 66dB$. These simulation results show that even low order (1^{st} or 2^{nd} order noise shaping) can provide enough error suppression.

It should be noted that the proposed technique does not suppress the thermal/flicker noise and the front-end DAC nonlinearity. The thermal/flicker noise and the DAC linearity requirements are the same as the conventional pipeline stage and it plainly benefits from oversampling. A form of dynamic element matching (DEM) such as the data weighted averaging (DWA) [16] may be used in the front-end DAC, similar to the traditional $\Delta\Sigma$ modulators.

As mentioned earlier, the MDAC settling error is also shaped in NSS. The settling requirement of the NSS can be compared with a conventional MDAC, operating at the Nyquist rate. The Nyquist MDAC amplifier needs to settle at least for $M \cdot ln(2)\tau$ second to achieve M-bit accuracy.

Hence, the transconductance (g_m) of the amplifier should satisfy the following constraint

$$M \cdot ln(2)\tau = M \cdot ln(2)\frac{C_L}{k \cdot g_m} < \frac{T_s}{2} \tag{6}$$

$$2M \cdot ln(2)\frac{C_L}{k \cdot T_s} < g_m \tag{7}$$

where C_L is the load of the MDAC, T_s is the sampling frequency/period and k is the feedback factor of the MDAC. The constraint in (7) remains unchanged, when the MDAC is oversampled, since both T_s and C_L are scaled by $\frac{1}{OSR}$ (the in-band thermal noise is scaled by OSR and the MDAC capacitors are scaled respectively).

In the NSS, the amount of settling error suppression depends on the order of NSS and the OSR. For instance, in a second order NSS settling error is at least 22 dB attenuated at 6X OSR. The amount of error attenuation for L^{th} order NSS can be derived from following equation.

$$(20L + 10)log(OSR) - 10log(\frac{\pi^2}{2L + 1}) \tag{8}$$

Hence, the MDAC settling time reduces to $(Mln(2) - 2.5)\tau$ for M-bit accuracy. Respectively, (7) can be rewritten as $\frac{2(Mln(2)-2.5)\cdot C_L}{k \cdot T_s} < g_m$ and the NSS amplifier needs less g_m (at 6X OSR) compared to the conventional Nyquist MDAC.

C. $\Delta\Sigma$ sub-ADC design requirements

The $\Delta\Sigma$ sub-ADC provides coarse quantization of the input signal. Any error generated by the $\Delta\Sigma$ sub-ADC appears at the digital output of the NSS stage. This error also appears at the residue output and consequently the digital output of the following stage. Hence, it is canceled out at the final digital output which is a weighted sum of the digital outputs of all stages. The sub-ADC errors are modeled as E_{SA} in Fig. 5 and following transfer functions shows how E_{SA} is canceled at the output

$$D_1 = H_F \cdot E_{SA} \tag{9}$$

$$D_2 = -G \cdot H_F \cdot E_{SA} \tag{10}$$

$$D_{out} = D_1 + \frac{D_2}{G} = 0 \tag{11}$$

E_{SA} represents any error generated by the $\Delta\Sigma$ sub-ADC including gain error, coefficient mismatch, thermal/flicker noise, and DAC nonlinearity in the $\Delta\Sigma$ sub-ADC. Hence, the $\Delta\Sigma$ sub-ADC has a very relaxed loop filter design requirements and can be implemented with minimal power dissipation and die area.

In summary, the design requirements of the sub-ADC in the proposed architecture are the same as the one in the conventional pipelined ADC. In a pipelined ADC with one-bit redundancy, the sub-ADC errors should be less than half-LSB and the same condition exists for the proposed architecture.

D. FIR filter design requirements

As mentioned earlier, the FIR filter plays an important role in NSS since it prevents opamp overload, reduces rms quantization power at the output and consequently suppresses nonlinear distortion power. The FIR filter should be chosen such that the magnitude of ($H_F \cdot NTF$) product does not exceed 0 dB over the (0 to $\frac{f_s}{2}$) frequency range. A good choice for the FIR filter is a semi-sinc filter with $\frac{(1+z^{-1})^N}{2^N}$ transfer function.

The minimum order of the FIR filter (N) should be the same as the order of the $\Delta\Sigma$ ADC to ensure that the magnitude of ($H_F \cdot NTF$) product is equal to or less than 0 dB and to avoid the opamp overload. The magnitude of the MDAC inter-stage gain is $|G \cdot H_F \cdot NTF|$ and by setting the maximum of $|H_F \cdot NTF|$ to one, the MDAC maximum gain remains the same as the conventional MDAC. Using a filter with higher order, compared to the order of the delta-sigma ADC, does not provide much benefit. Although it provides better out-of-band noise shaping, it increases design complexity. However, other filter choices, which would provide a similar set of properties, can also be used in the proposed architecture.

Although identical FIR filters are intended to be used in the signal and the sub-ADC paths, matching between the filters is not critical. A fraction of the input signal (V_{in} in Fig. 1) appears at the MDAC output as a result of the mismatch between the two FIR filters. This will only increase the MDAC output swing and change the input signal transfer function (STF) slightly without degrading the overall performance. However, if the mismatch between the two filters is very large, the extra MDAC swing, resulting from the mismatch between filters, may overload the amplifier. In a 3.5-bit NSS, the mismatch between the DAC and signal filters can be tolerated to approximately 6 percent. This mismatch constraint can be easily satisfied via a capacitor network to implement the filters.

The low-pass transfer function of the FIR filter contains several delaying terms ($H_F = A_0 + A_1 z^{-1} + A_2 z^{-2} + ...$). The weighted sum of the filter coefficients ($A_0 + A_1 + ...$) should be accurate enough since it determines the inter-stage gain. However, the mismatch between coefficients

(A_1, A_2,...) mildly changes the location of the zeros of the filter and slightly degrades the high frequency noise shaping, as shown in Fig. 6. In this figure, the ideal first order transfer function ($H_F \cdot NTF$) is compared to a case with random 10 and 20 percent mismatch between filter coefficients. Although high frequency noise shaping is degraded, the maximum magnitude of the $H_F \cdot NTF$ changes only slightly (0.2dB) even for such large (far more than realistic) coefficient mismatches. Hence, the coefficients have very relaxed matching requirements. Passive realization of the FIR filter with minimum power penalty is possible. The delaying terms of H_F can be generated by sampling the input signal in the alternate clock phases. The complexity of the SC network (realizing the coefficients of the FIR filter) is minimal for first and second order architectures.

In summary, the above techniques, using a low power coarse $\Delta\Sigma$ sub-ADC and a passive FIR filter, improve the linearity of the front-end MDAC significantly.

III. Proposed Noise-Shaped Pipelined ADC

The NSS may be used as the front-end stage(s) of an oversampled pipelined ADC to improve linearity. In this section, efficient implementation for the back-end is studied and the architecture details of the proposed pipelined ADC is presented.

A. Noised-shaped back-end architecture

High resolution pipelined ADCs usually use a large number of pipelined stages to reduce the quantization noise sufficiently. Although the power dissipation and the die area of the back-end stages could be scaled, using many pipelined stages is not power/area efficient, especially in oversampling applications where noise shaping could be applied to reduce the amount of in-band quantization noise, even at low OSRs.

The Noise Shaped Two-Step (NSTS) ADC, introduced in [15], exploits residue feedback and capacitor/opamp sharing to achieve noise shaping with minimal design complexity. This architecture does not require additional active elements (e.g. opamp, comparator) to achieve noise shaping. Simulation results indicate that NSTS ADC can suppress in-band quantization noise by more than 20dB even at a very low OSR (e.g. 6X OSR). This is equivalent to using 2-3 extra pipelined back-end stages.

The architecture of NSTS back-end ADC is shown in Fig. 7. In this architecture, a multiplying-DAC (MDAC) is added to the second stage (rather than having just the quantizer) to extract the final stage's quantization noise. This quantization noise (analog residue) is fed back to the input of ADC with the transfer function $H(z)$. The signal provided by this feedback path provides noise shaping for the quantization noise of the final stage (E_2). The feedback path can be configured to provide the desired order of noise shaping. The residue amplifier of this two-step ADC may be shared between the two MDACs. Hence, no extra amplifier would be required to achieving noise shaping.

The NSTS ADC is prone to the first stage quantization noise leakage. E_1 needs to be canceled out at the output, but inaccurate inter-stage gain can make the cancellation imperfect. However, the quantization noise leakage is less of a concern when NSTS is used as the back-end of an oversampling ADC, since the leakage of the back-end stages is suppressed by the inter-stage gain of the front-end stages.

B. Proposed pipelined ADC

The proposed noise-shaped pipelined ADC is shown in Fig. 8. The first two front-end stages are NSS and the back-end ADC is a noise-shaped two-step (NSTS) ADC. The front-end stages resolve the MSBs (3-bits each stage). The back-end NSTS ADC generates the LSBs and provides noise shaping for the final quantization. The NSTS ADC resolves 5-bits with third-order noise shaping. The pipelined ADC resolves a total of 9-bits. The very first stage of the pipelined ADC is a second-order NSS while the second stage is a first-order NSS, since the second stage does not need to be as accurate as the first. An amplifier is shared between these two front-end stages. The NSTS ADC also requires only one amplifier for the two-step quantization with a third-order noise shaping.

In the traditional pipelined ADCs, the final digital output is a scalar weighted sum of the digital output. In the proposed architecture, the digital output of the first and the second stages should be applied to a product $H_{F1}H_{F2}$ and a single H_{F2} digital filters, respectively, and added with the digital output of the band-end NSTS ADC. This will appropriately cancel out the quantization of all the stages involved. The digital output (D_i) and the output residue (X_{ri}) of all stages may

be found as follows:

$$D_1 = V_{in} + NTF_1\ E_1 \tag{12}$$

$$X_{r1} = -G_1\ H_{F1}\ NTF_1\ E_1\ z^{-0.5} \tag{13}$$

$$D_2 = X_{r1} + NTF_2\ E_2 = -G_1\ H_{F1}\ NTF_1\ E_1\ z^{-0.5} + NTF_2\ E_2 \tag{14}$$

$$X_{r2} = -G_2\ H_{F2}\ NTF_2\ E_2\ z^{-0.5} \tag{15}$$

$$D_3 = X_{r2} + E_3 - H(z)\ E_4\ z^{-0.5} = -G_2\ H_{F2}\ NTF_2\ E_2\ z^{-0.5} + E_3 - H(z)\ E_4\ z^{-0.5} \tag{16}$$

$$X_{r3} = -G_3\ E_3\ z^{-0.5} \tag{17}$$

$$D_4 = X_{r3} + E_4 = -G_3\ E_3\ z^{-0.5} + E_4 \tag{18}$$

$$\begin{aligned} D_{out} &= H_{F1}\ H_{F2}\ D_1\ z^{-1.5} + \frac{H_{F2}\ D_2\ z^{-1}}{G_1} + \frac{D_3\ z^{-0.5}}{G_1\ G_2} + \frac{D_4}{G_1\ G_2\ G_3} \\ &= H_{F1}\ H_{F2}\ V_{in}\ z^{-1.5} + \frac{NTF_4\ E_4}{G_1\ G_2\ G_3} \end{aligned} \tag{19}$$

$$NTF_4 = 1 - G_3\ H(z)\ z^{-1} \tag{20}$$

Here, E_i, G_i, NTF_i and H_{Fi} represent the quantization noise, inter-stage gain, noise transfer function and filter transfer function of the i^{th} pipeline stage. In the final digital output, shaped quantization of only the last stage (E_4) appears. $E_4/(G_1\ G_2\ G_3)$ represents the quantization of the 9-bit ADC. A third-order noise shaping is provided by NTF_4, which boosts the resolution of the ADC to 13-bits with just a small amount of oversampling (6X OSR). Note that the front-end stages of the ADC work independently of the back-end NSTS ADC, and hence, front-end stages have no role in forming the final noise transfer function (NTF_4). In other words, the internal noise shaping of the front-end stages (NTF_1 and NTF_2) is intended only to reduce the front-end imperfections/nonlinearities.

The SQNR (signal to quantization noise ratio) of the oversampled ADCs can be estimated from following equation [13]

$$SQNR_{max}[dB] = 6.02M + 1.76 + (20(L) + 10)log_{10}(OSR) - 10log_{10}(\frac{\pi^{2(L)}}{2(L)+1}) \tag{21}$$

where M is the number of bits resolved in the oversampling ADC and L is the order of noise shaping. In the proposed ADC, M is 9; L is 3 and OSR is 6. Hence, the maximum achievable SQNR is 88 dB which is more than enough for the desired 13-bits accuracy.

The input signal transfer function ($H_{F1}\ H_{F2}\ z^{-1.5}$) is a low pass FIR filter which is expressed as follows:

$$H_{F1}\ H_{F2} = \frac{(1+z^{-1})^{N_1+N_2}}{2^{N_1+N_2}} \tag{22}$$

Here, N_1 and N_2 are the orders of the NSS stages (2 and 1 in this implementation). This will yield a third order low-pass filtering with three zeros at $f_s/2$. The in-band attenuation of the filter is not significant even at very low OSRs (less than 1dB at 6X OSR).

C. Proposed architecture design requirements

The errors generated by the pipelined stages appear differently at the output. As mentioned in section II.B, the inter-stage gain error (E_{r1}) of the NSS is shaped. The shaped error of the first NSS appear directly at the output of the proposed pipelined ADC. The inter-stage error of the second stage (E_{r2}) is shaped and also suppressed by G_1. E_{r3} and E_{r4} from the NSTS ADC are not shaped but scaled by the inter-stage gains of the preceding stages. Hence, the inter-stage gain errors of all pipelined stages are either shaped or suppressed, thus all MDACs have relaxed design requirements. These errors are modeled in Fig. 9. It should be noted that E_{ri} includes any error that makes the inter-stage gain inaccurate (e.g. opamp gain error, settling error and capacitor mismatch).

Thermal noise requirements of the pipelined stages is same as the traditional pipelined ADCs. The thermal noise of the first stage directly appears at the output and noise from other stages is suppressed by the inter-stage gains of the preceding stages. The overall thermal noise is scaled by the OSR.

IV. ADC Circuit Realization

The circuit realization of the proposed architecture will be discussed in this section. Several techniques are employed to simplify the SC implementation of the NSS and the back-end NSTS. These techniques together improve the power efficiency and reduce the area consumption.

A. NSS circuit realization

Fig. 10 shows a simpler version of the NSS implementation with a first-order $\Delta\Sigma$ loop and a passive first-order filter. In this realization, separate sampling and DAC capacitors are used.

The transfer function of the first-order filter is $H(z) = 0.5 + 0.5z^{-1}$. This filter is realized in the input signal path by dividing the sampling capacitor into smaller ones; one of them (C_A) represents the 0.5 term in $H(z)$, and the set of capacitors (C_{B1} and C_{B2}) realizes the delayed term $(0.5z^{-1})$. The total sampling capacitance used ($C_A + C_{B1,2}$) is same as a conventional pipeline stage. The capacitors C_{B1} and C_{B2} sample the input voltage in alternate clock phases (phase-1a and phase-1b), and the stored charge is used with a one cycle delay. Mismatch between C_{B1} and C_{B2} changes the signal transfer function in the alternate clock phases, and generates an undesired image at frequencies close to f_s/2. However, due to oversampling, this image will be outside the signal band. Hence, the matching between the input sampling capacitors is not a concern.

The main challenge in the design of NSS is the realization of the low-pass filter in the sub-ADC path without increasing the number of DAC unit elements. The straightforward implementation of a first-order filter ($H(z) = 0.5(1 + z^{-1})$) would be to use one set of DAC unit elements for each filter term. For a B-bits quantizer, this approach would require a front-end DAC with $2 \cdot 2^B$ unit elements. This is undesirable. Hence, the filter in the sub-ADC path is further optimized. The output words of the sub-ADC are delayed in the digital domain to realize the delaying terms in $H(z)$. One set of DAC unit elements are used to process both the current and the delayed digital output of the sub-ADC as follows. During the phase-1 cycle, the reference values corresponding to the delayed samples are stored on the DAC capacitors. During the next phase-2 cycle, the DAC is connected to the opamp, and the current digital output applies the reference voltages to the DAC. Thus, the resulting number of the DAC unit elements is 2^B, which is equal to the traditional pipeline stage.

The proposed circuit realization does not limit the operation frequency, since the total capacitance required in the proposed scheme remains the same as conventional MDAC and the feedback factor remains unchanged.

In this prototype design, both types (second and first order) of NSS are used. The second order NSS is shown in Fig. 11. The transfer function of the second-order filter is $H(z) = 0.25(1 + 2z^{-1} + z^{-2})$. An accurate 5-level DAC unit element is devised to keep the number of unit elements for this second order NSS unchanged (2^B unit elements for B-bit quantizer). Similar to the first-order NSS, reference values (V_{r+} or V_{r-}) corresponding to z^{-1} term are stored on the DAC capacitors in phase-1. During the next cycle phase-2, the sum of the current

and the two-cycle delayed digital output $(1 + z^{-2})$ is applied to the reference voltages of the DAC. Note that $(1+z^{-2})$ addition doubles the number of the output word. A 3-level reference is used in phase-2 to address this. Hence, each DAC unit element resolves 5-levels, two levels in phase-1 and three levels in phase-2. The second-order filter in the signal path is also realized via splitting the sampling capacitor into smaller parts which sample the input signal in the alternate clock phases similar to the first-order architecture.

Although the gain requirement of NSS is relaxed (about 40dB), a two-stage amplifier (shown in Fig. 12) is employed in the front-end NSS to provide enough output voltage swing. The first stage of the amplifier is a half-telescopic differential pair (only NMOS pair is cascoded), which is well suited for the low voltage operation. A simple resistive common-mode feedback (CMFB) is used for both stages of the amplifier and a current source (I_{cm}) is added to the second-stage CMFB [7] for the fine trimming of the output common mode voltage. Because both the input and output common-mode voltages are set to half-Vdd, the sampling switches have a limited gate-source overdrive voltage. Hence, left and right side switches of the front-end NSS are bootstrapped [17] to reduce switch on-resistance and to increase the operation speed.

B. DAC linearity improvement

In the SC gain stages, mismatches in the DAC unit elements cause harmonic distortion. Such DAC non-linearity leads to even as well as odd harmonics. Even harmonics appear at the output, because the random mismatch errors corresponding to each of the digital codes do not scatter symmetrically around the mid-code. In a multi-bit DAC, each unit element may be modeled as having the value $u_j = U + d_j$ (for $j = 1, 2, ..., 2M$) where U is the average unit element and d_j is the deviation of u_j from the average. Note that sum of all errors $\sum_{j=1}^{2M} d_j = 0$, since the average unit element $U = \sum_{j=1}^{2M} \frac{u_j}{2M}$. The mid-code is M and DAC errors are distributed asymmetrically (i.e. randomly) because the absolute mismatch error for code $M + i$ ($E_{M+i} = \sum_{j=1}^{M+i} d_j$) is different (in magnitude) from the mismatch error for code $M - i$ ($E_{M-i} = \sum_{j=1}^{M-i} d_j$).

In the proposed NSS architecture, the DAC unit elements are shared between the current and the delayed digital output. Given such usage of common elements for both the current and the delayed output, the even harmonics, which is caused by DAC non-linearity, can be avoided

simply by establishing a common centroid *selection* of the unit elements as shown in Fig. 13. In this scheme, codes 1-2M are applied to the unit elements 1-2M in ϕ_1, while inverse codes (opposite direction) 2M-1 are applied to the unit elements 1-2M in ϕ_2. The average error for each of the codes (at $M+i$ an $M-i$) are

$$E_{M+i} = 0.5(\sum_{j=1}^{M+i} d_j + \sum_{j=M-i+1}^{2M} d_j) = 0.5(\sum_{j=1}^{2M} d_j + \sum_{j=M-i+1}^{M+i} d_j) = 0.5 \sum_{j=M-i+1}^{M+i} d_j \qquad (23)$$

$$E_{M-i} = 0.5(\sum_{j=1}^{M-i} d_j + \sum_{j=M+i+1}^{2M} d_j) = 0.5(\sum_{j=1}^{2M} d_j - \sum_{j=M-i+1}^{M+i} d_j) = -0.5 \sum_{j=M-i+1}^{M+i} d_j \qquad (24)$$

It is apparent from these expressions/derivations that the errors are distributed symmetrically (equal in magnitude and opposite in polarity) in this scheme. In other words $E_{M-i} = -E_{M+i}$. Hence, the even order harmonics (dominant portion of the total harmonics) are avoided. A simple 5-elements example of the common-centroid bit assignment technique is shown in Fig. 14. This figure illustrates the symmetric error distribution. Fig. 15 shows the simulated output spectrum of NSS before and after applying the proposed common-centroid selection scheme. For one percent random mismatch among the DAC unit elements, the proposed scheme eliminates even harmonics and improves SFDR by about 13dB. Note that one percent arbitrary mismatch is considered between DAC unit elements to demonstrate the effectiveness of the proposed technique. This is very useful for low OSR applications where DEM techniques are not very effective. In the implemented prototype, a very simple one-bit scrambler is added to this common-centroid selection scheme to suppress the odd harmonics as well. This technique can be similarly extended to the second order NSS.

C. $\Delta\Sigma$ sub-ADC design

The $\Delta\Sigma$ modulator in the NSS is used only in the coarse quantization of the input signal, thus it has much relaxed accuracy requirements. Hence, it may be implemented with a very low power consumption. A new design scheme is incorporated into this prototype to simplify the $\Delta\Sigma$ sub-ADC and to further reduce power consumption.

In the prototype ADC, a second-order and a first-order $\Delta\Sigma$ sub-ADCs are used in the first and the second MDACs. The conventional feedforward structure is used in the first-order sub-ADC, but the design of the second-order sub-ADC had to be further simplified. The system

level realization of the feedforward second-order $\Delta\Sigma$ sub-ADC incorporating a new second-order integrator is shown in Fig. 16. This second order system requires only one amplifier and simplifies signal addition at the input of the quantizer. This is a much simpler solution compared to the conventional feedforward structure [26].

The circuit realization of the second-order integrator is shown in Fig. 17. In this circuit, the sampled input signal is first integrated in phase-2. During this phase, the sampled charge on C_1 is transfered to C_2 and added with the previously held voltage on C_2 , similar to the conventional Switched Capacitor (SC) integrator. During the same phase, the capacitor network (C_3, C_4 and C_5) also samples the opamp output voltage ($C_2 = C_3 = C_4 = C_5$). Then the sampled output voltage is re-integrated in phase-1 and fed to the quantizer. The capacitor network (C_3, C_4 and C_5) works as an additional feedback path around the integrator and the whole SC circuit represents a second-order integrator. Capacitors C_4 and C_5 sample the signal in the alternate clock phases to generate an extra delay in the integration (required for the second order system). Note that mismatch between C_4 and C_5 can fold the quantization noise in the signal band. However, the noise folding is not a concern since the delta-sigma sub-ADC needs to be only around 4-bit accurate and good matching (e.g. 1-2 percent) between C_4 and C_5 can be easily achieved.

The feeback factor of the second-order integrator is the same as conventional integrator in phase-2, but it is 33 percent lower than conventional integrator in phase-1. However, the feedback factor degradation will not increase the overall power consumption since the proposed architecture requires one less amplifier.

In the CMOS process we used for this prototype, the minimum available unit capacitor available was around 10 fF, and using 9-level switched capacitor (SC) DAC in the $\Delta\Sigma$ sub-ADC would have made the total sampling capacitor of about 90 fF. However, because the $\frac{KT}{C}$ noise requirements of the $\Delta\Sigma$ sub-ADC is much relaxed, a resistor ladder front-end DAC was used instead. And the resistor DAC is shared with the reference generator of the flash quantizer. The much relaxed accuracy requirements of $\Delta\Sigma$ sub-ADC allows this simplification. The power consumption of the amplifier used in the $\Delta\Sigma$ sub-ADC (shown in Fig. 18) is about 200μW, which is less than two percent of the total ADC power consumption. The area consumption of the loop filter is also less than two percent of the total chip area.

D. Back-end NSTS implementation

The design of NSTS ADC was discussed in the previous section. A third-order NSTS ADC is used as the back-end of the noise-shaped pipelined ADC. The feedback path $H(z)$ (Fig. 7) has three terms and all these terms should normally be added at the input. This implies switched capacitor network for both the MDAC input as well as the quantizer input. In order to simplify the signal addition at the input of the quantizer, only the A_1 feedback path is added at the input of the NSTS quantizer. This modification directly injects error into the quantizer input. However, the 3-bits resolved in the last stage keeps the feedback residue small and the built-in digital redundancy absorbs this error.

The circuit realization of the third order NSTS is shown in Fig. 19. The opamp/capacitor sharing scheme, introduced in [15], is employed in the back-end NSTS ADC. This scheme shares the feedback capacitor (C_c) and the residue amplifier between the two stages of NSTS. In phase-1, the SC circuit works as the first MDAC. The charge that was stored on C_c in the preceding phase-2 takes the role of the feedback path A_1. In phase-2, the gain stage operates as the second stage where C_c is the flip-around sampling capacitor. The output residue voltage of the gain stage in phase-1 is X_{r3} and in phase-2 is X_{r4}. Note that the output signal of the amplifier is not integrated through the feedback path. This is because the output voltage of the amplifier is quantized in phase-1 and the output voltage memory is wiped out in the succeeding phase-2. A more detailed operation of this opamp/capacitor sharing technique is found in [15]. This technique reduces the design complexity and the output loading of the amplifier, since C_c simultaneously plays the role of the sampling capacitance and the output load.

As mentioned earlier, the feedback paths A_2 and A_3 are also added at the input of the second NSS stage (i.e. included in the MDAC path). The delay in these paths is implemented by using a sampling capacitor network and transferring the signal in alternate clock phases.

A two-stage amplifier (shown in Fig. 20) is used for the back-end NSTS to provide enough output swing. The low gain requirement of the NSTS eliminates the need for the cascoded devices in the first-stage. PMOS input pair is used to accommodate near-ground common-mode voltage (≈0.3 V) and non-bootstrapped NMOS switches in the NSTS.

V. Measurement Results and Conclusions

The proposed noise-shaped pipelined ADC was designed and fabricated in a 2P4M 0.18μm CMOS process [19]. The die photograph is shown in Fig. 21. The total active die area is 1.2 mm^2.

A test option was implemented to disable the loop filter in the $\Delta\Sigma$ sub-ADCs to compare the effectiveness of the proposed NSS. The sub-ADC becomes a regular flash sub-ADC and the properties of the front-end stage becomes similar to the traditional pipeline stage when the loop filter is disabled. The loop gain of the amplifier used in the front-end stage is about 45dB based on simulation.

The measured output spectrum is shown in Fig. 22 and Fig. 23 for 64 MHz sampling rate before and after activating the $\Delta\Sigma$ sub-ADCs. At 6X OSR, the peak SNDR and SFDR are improved 15dB and 26dB, respectively, when the $\Delta\Sigma$ of NSS is activated. These properties are well matched to the simulation results given in section II. The power dissipation of the loop filter in each $\Delta\Sigma$ sub-ADC is only 200μW. The total analog and digital power consumptions of the entire prototype IC are 8.2mW and 5.7mW, respectively. The SNDR plot versus input signal amplitude is shown in Fig. 24 for 64 MHz sampling rate with 6X OSR. The FOM of this prototype is compared with the state-of-the-art 11-13 bits (Nyquist and oversampling) ADCs with the conversion rates of 1 to 25 MHz in Fig. 25 [20].

Acknowledgment

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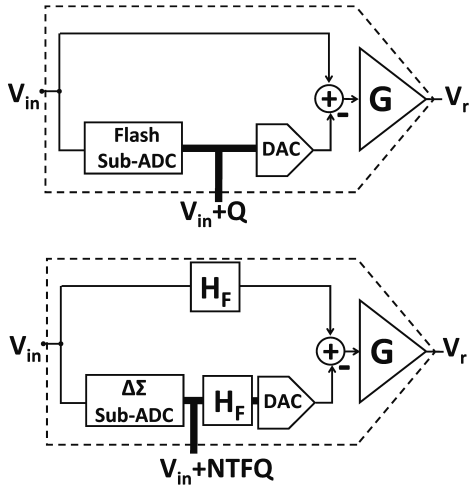

Fig. 1. Front-end of a pipelined ADC: a) conventional stage; b) proposed noise-shaped pipeline stage (NSS)

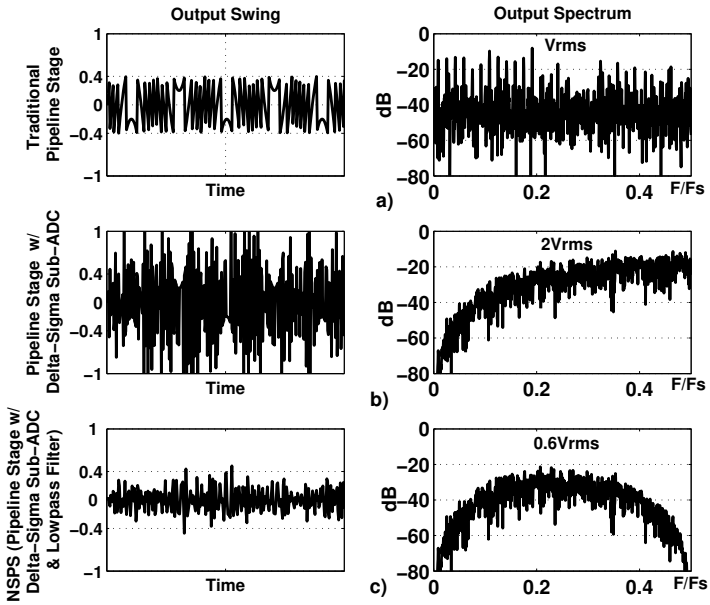

Fig. 2. The MDAC output voltage and spectrum: a) Traditional pipeline stage; b) Pipeline stage w/ $\Delta\Sigma$ sub-ADC and without low-pass filter c) The proposed NSS utilizing both $\Delta\Sigma$ sub-ADC and low-pass filter

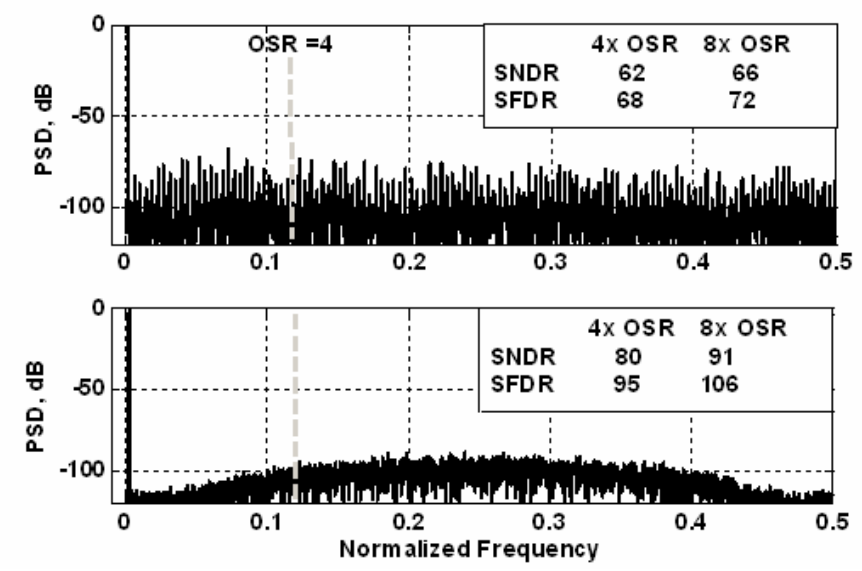

Fig. 3. Output spectrum of ADC with traditional and NSS front-end stages (Nonlinear gain is assigned to opamp)

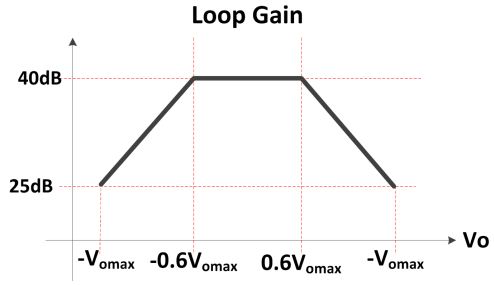

Fig. 4. Gain of the opamp used in Fig. 3 vs output swing of the opamp

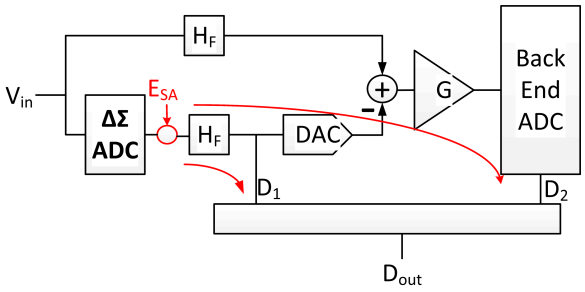

Fig. 5. Modeling sub-ADC errors in NSS

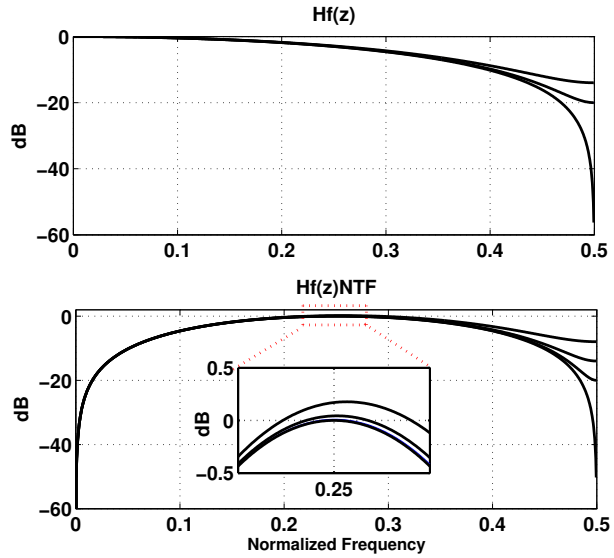

Fig. 6. Variation due to random mismatch among filter coefficients

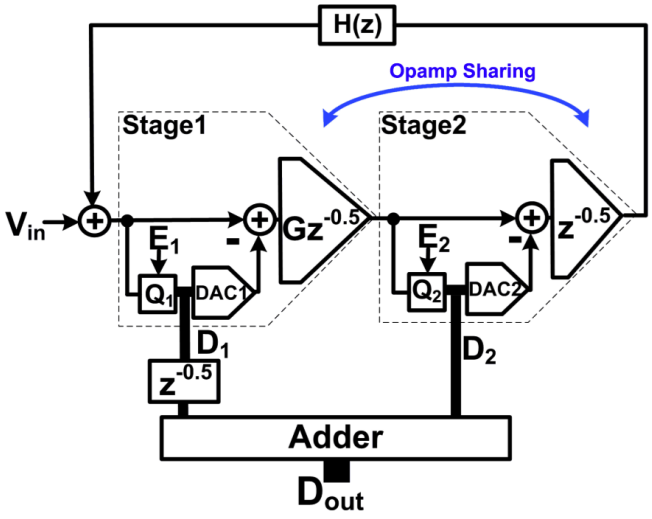

Fig. 7. The Noise-Shaped Two-Step (NSTS) back-end ADC

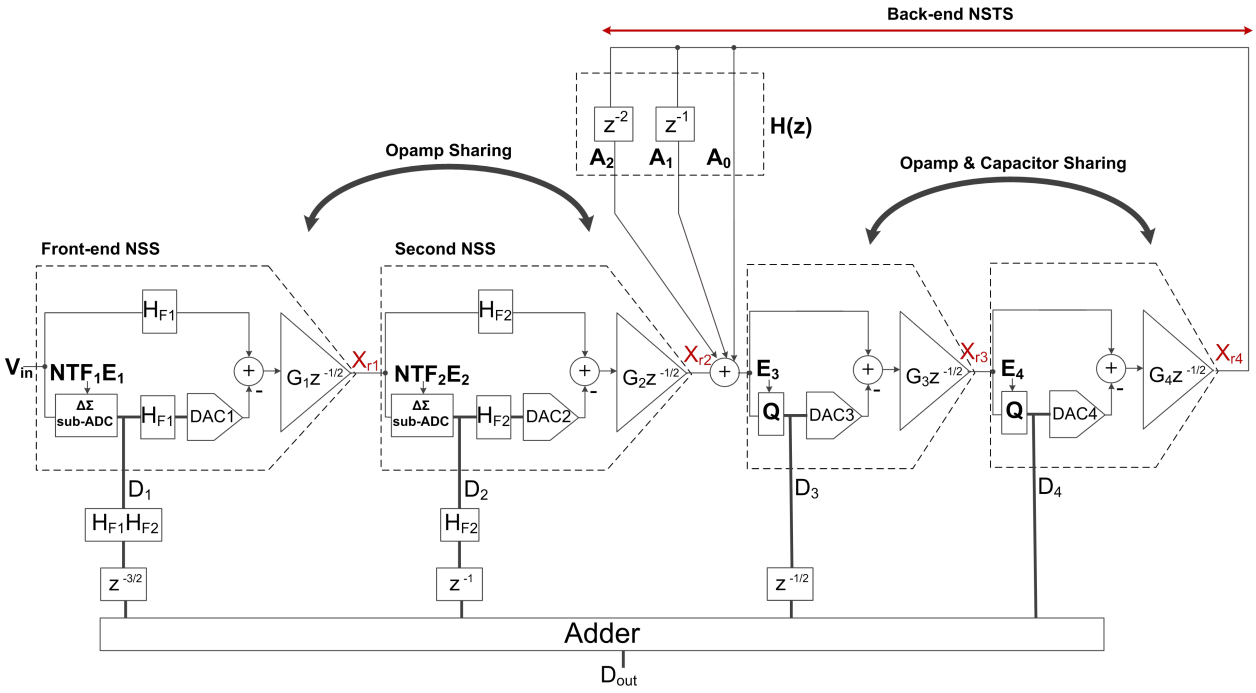

Fig. 8. The proposed noise-shaped pipelined ADC

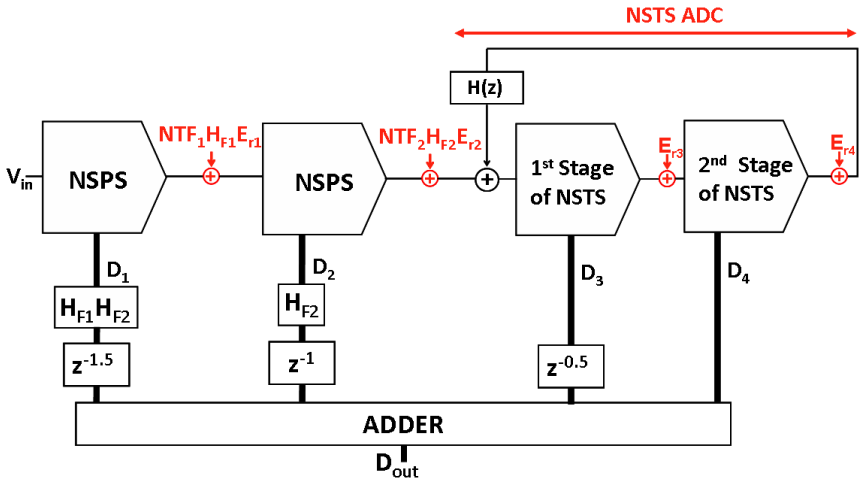

Fig. 9. Modeling inter-stage errors in the proposed architecture

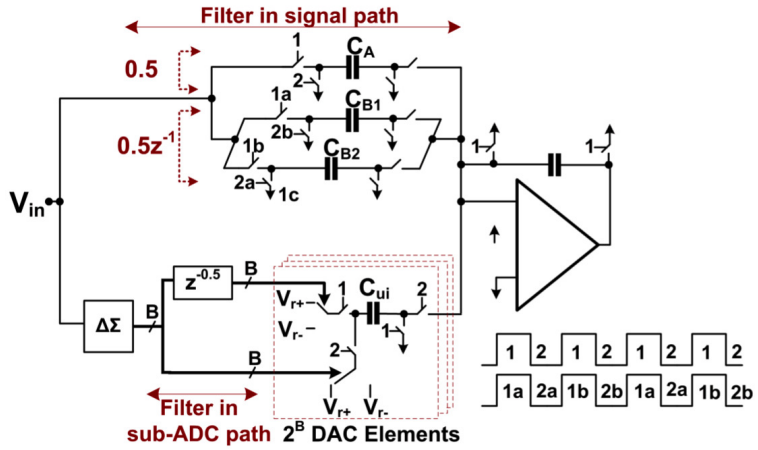

Fig. 10. The circuit realization of the first-order NSS

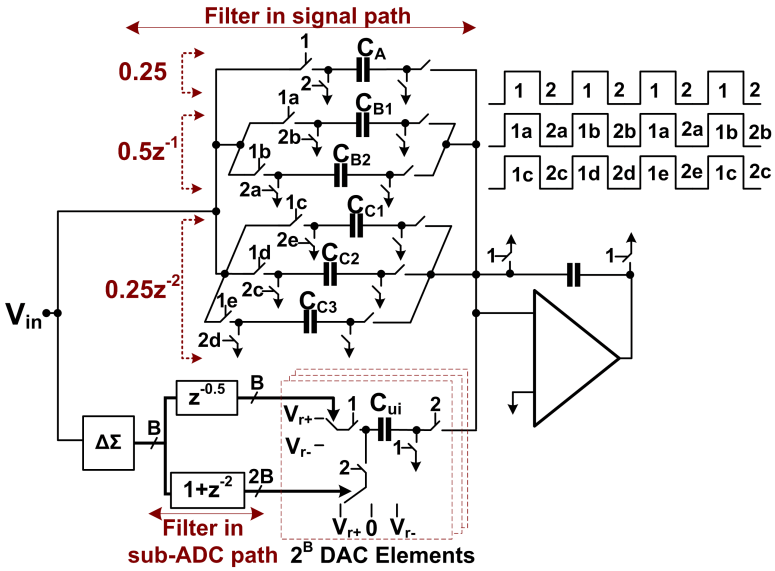

Fig. 11. The circuit realization of the second-order NSS

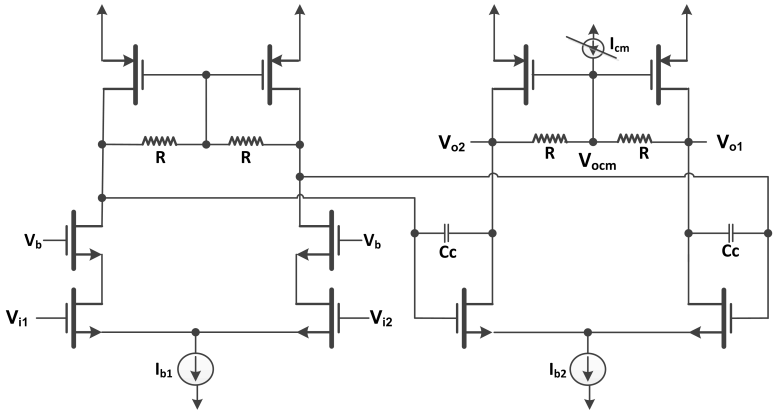

Fig. 12. The amplifier used in NSS

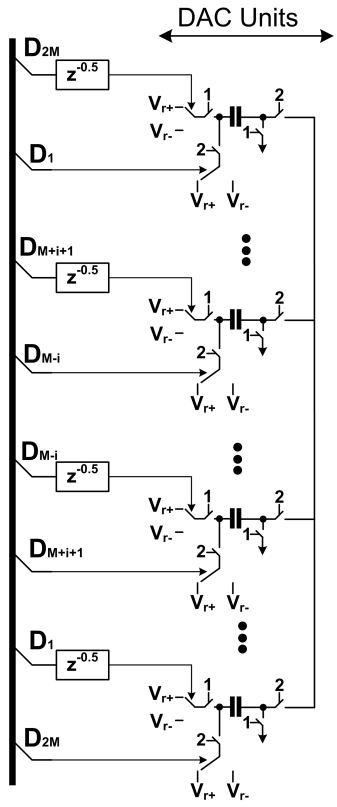

Fig. 13. The common centroid selection of DAC unit elements

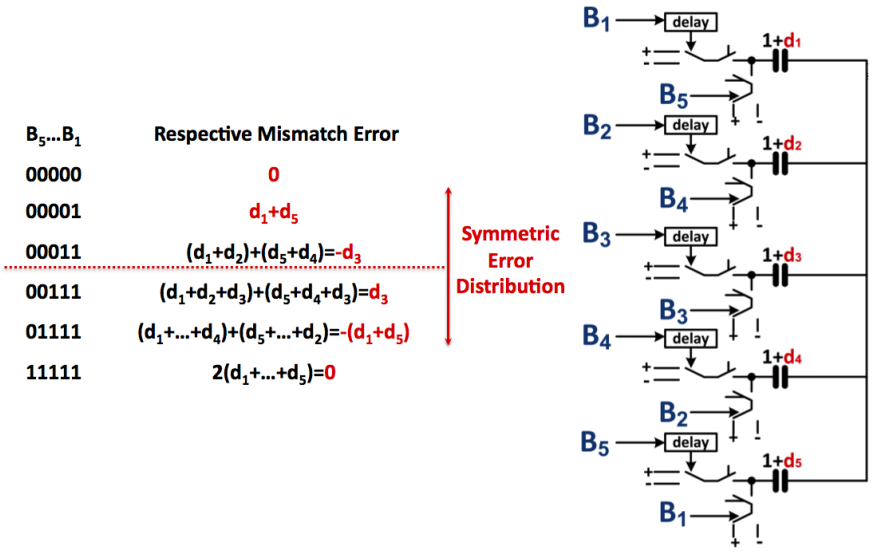

Fig. 14. The common centroid selection of DAC unit elements (5 unit elements example)

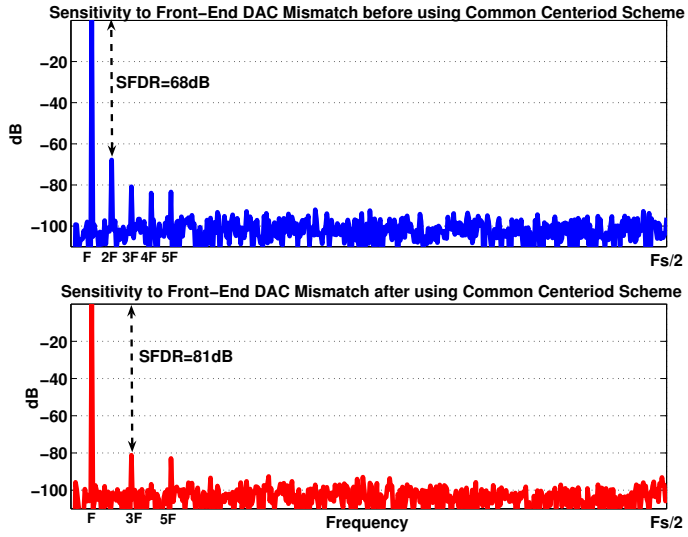

Fig. 15. The DAC nonlinearity suppression achieved by using common centroid scheme

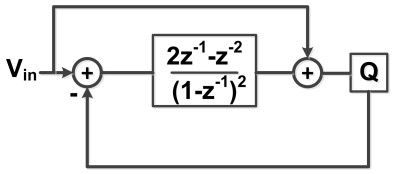

Fig. 16. The system level realization of the second-order $\Delta\Sigma$ sub-ADC

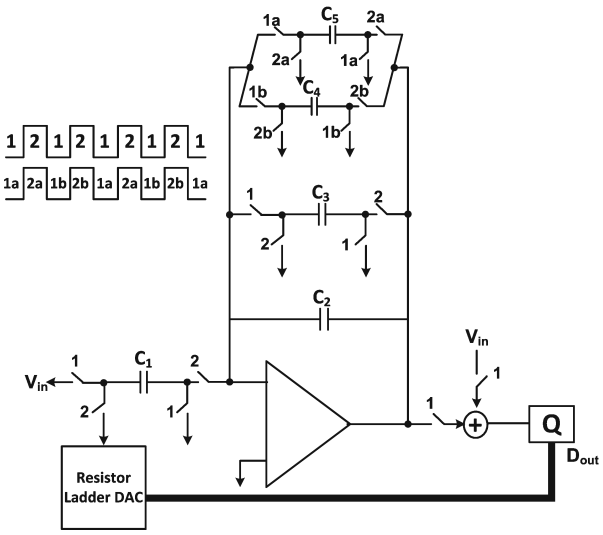

Fig. 17. The circuit level realization of the second-order $\Delta\Sigma$ sub-ADC

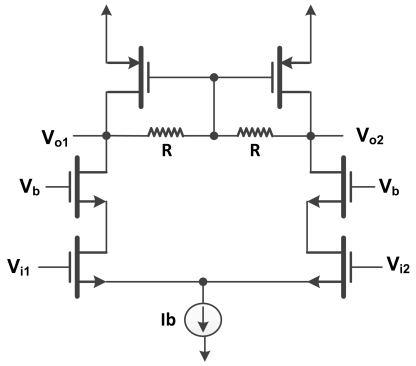

Fig. 18. The amplifier used in $\Delta\Sigma$ sub-ADC

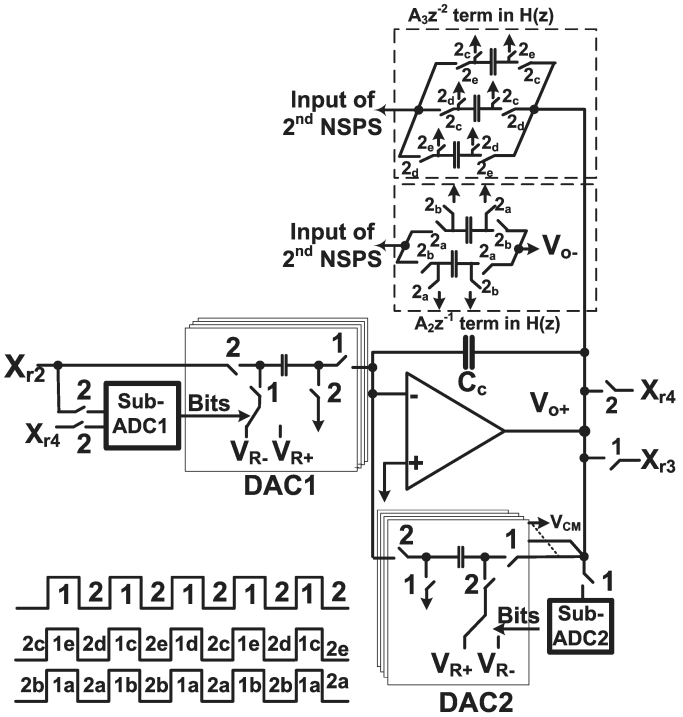

Fig. 19. The circuit realization of the back-end NSTS ADC

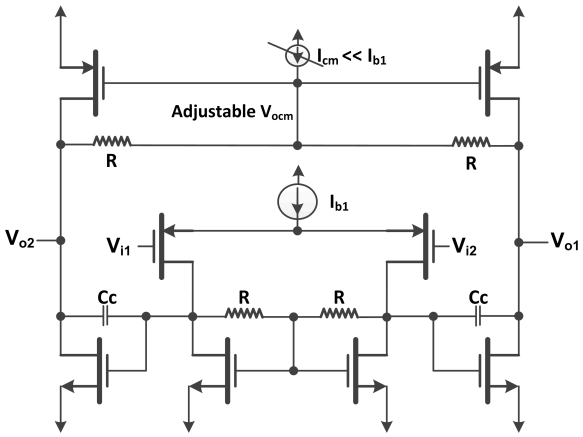

Fig. 20. The amplifier used in NSTS

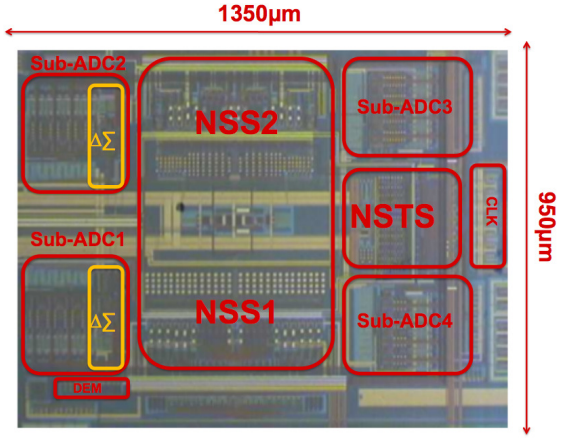

Fig. 21. Die micrograph (0.18μm CMOS)

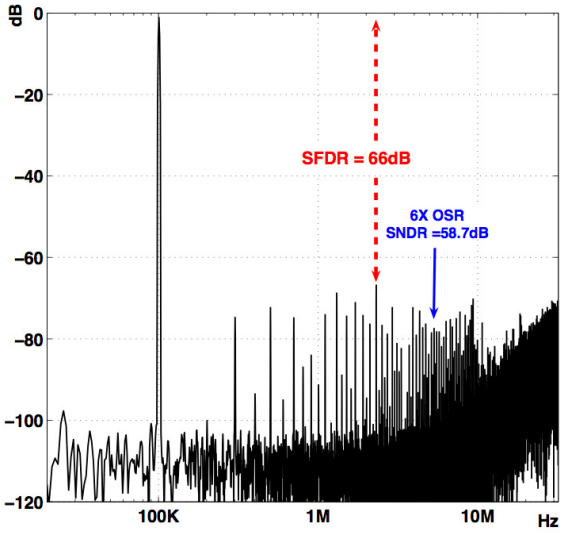

Fig. 22. The output spectrum of the ADC without NSS activated

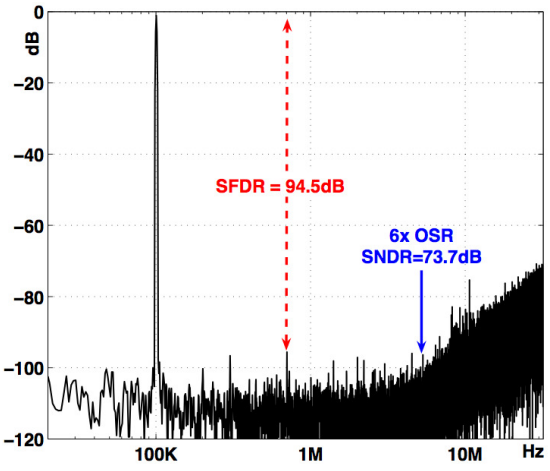

Fig. 23. The output spectrum of the ADC with NSS activated

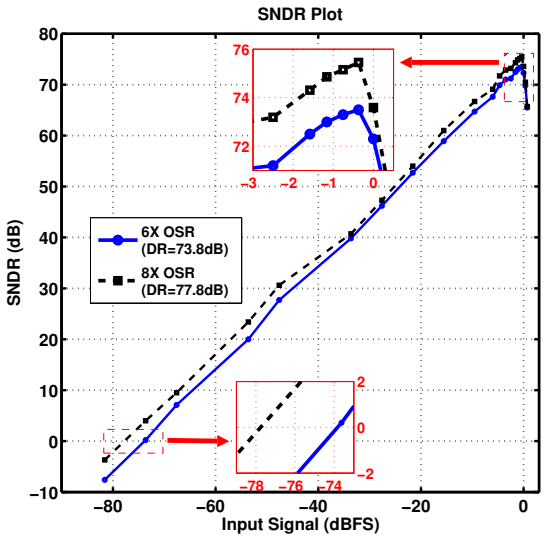

Fig. 24. The SNDR plot for 8X and 6X OSR

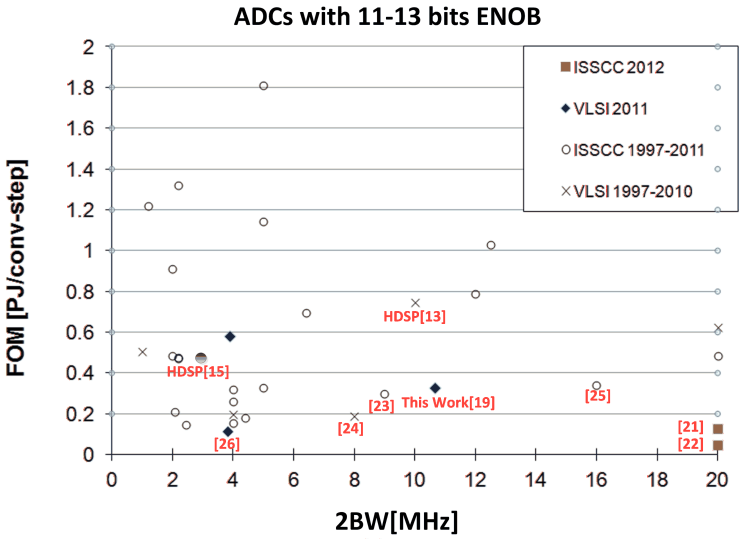

Fig. 25. ADC Performance survey

TABLE I

SUMMARY OF THE MEASUREMENT RESULTS

Sampling Rate	**64 MHz**
Signal Bandwidth	**5.33 MHz**
OSR	**6**
SFDR (dB)	**94.5**
DR (dB)	**73.8**
SNDR (dB)	**73.7**
Input Range (Diff)	**2.2 Vpp**
Comparator Reference voltage	**1.2 V**
Analog Supply(V)	**1.3**
Digital Supply(V)	**1.55**
Analog Power	**8.2mW**
Digital Power	**5.7mW**
FOM	**0.27pJ/conv-step**
Core Area (0.18μm CMOS)	**1.2** mm^2