

Digital excess loop delay compensation technique with embedded truncator for continuous-time delta-sigma modulators

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A novel implementation is proposed to relax the specifications of the internal feedback path for a continuous-time delta-sigma modulator. A truncator is embedded into the digital excess loop delay (ELD) compensation path. Thermometer-coded truncation is achieved by re-ordering the reference voltages of the internal quantiser. This requires only a small amount of extra digital circuitry compared to the conventional digital ELD compensation. The digital encoder controlling the digital-to-analogue converter is simple, and it only introduces a small ELD.

Introduction: In communication systems, rapidly increasing demands on system bandwidth lead to design challenges for the analogue front end. High-speed high-performance analogue-to-digital converters thus became necessary. The continuous-time delta-sigma ($\Delta\Sigma$) modulator (CT-DSM) is a good candidate due to its mid-to-high resolution, high speed and its intrinsic anti-aliasing filter. Recent work has raised the sampling rate to the gigahertz range in CT-DSMs [1], using advanced processes.

When a high sampling rate is used, the excess loop delay (ELD) caused by the regeneration time of the internal quantiser and of the control circuit in the internal feedback path including dynamic element matching (DEM), impairs the modulator's stability. Hence, ELD compensation has become essential in high-speed CT-DSM design [2]. To avoid the design difficulty in the analogue domain, several authors implemented ELD compensation in the digital domain [1–3]. As shown in Fig. 1a, the ELD compensation path can be realised entirely in the digital domain [3]. The structure described in [2] requires more comparators and DAC levels; the compensation can also be realised by shifting the reference levels of the internal quantiser as shown in Fig. 1b [1].

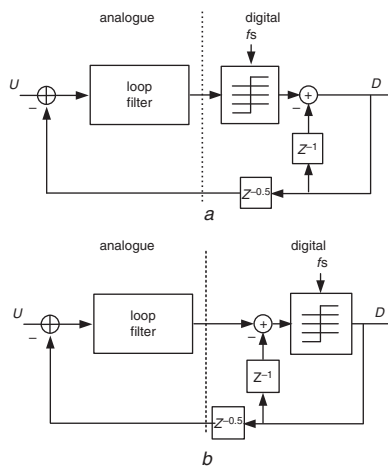


Fig. 1 Digital ELD compensation

a Fully digital implementation [3]
b Reference level shifting in internal quantiser [1, 2]

Another design challenge in high-speed CT-DSMs concerns the internal multi-bit feedback DAC. DEM circuitry is usually introduced to randomise and filter the unit element mismatch errors in the DAC. This may cause a larger ELD. Alternatively, digital calibration techniques can be used, but this results in more complexity. Hence, the internal DAC implementation becomes a bottleneck in CT-DSM design. Furthermore, the resolution of the DAC limits the internal quantiser resolution.

To allow high resolution for the internal quantiser, a digital $\Delta\Sigma$ truncator can be utilised to decrease the number of the output levels while shaping the truncation error [4]. However, the truncator may also introduce an extra delay due to the digital adder, which limits its use to relatively low sampling rates.

Proposed scheme: In this Letter, a low latency $\Delta\Sigma$ truncation circuit is proposed. The feedback path in the truncator is merged with the ELD

compensation path controlling the reference selection of the internal quantiser. The proposed scheme embeds the truncator within the digital ELD compensation path without added circuit complexity. The encoder of the DAC control logic only introduces a small delay. Hence, the proposed topology is suitable for implementation even at very high sampling rates.

The proposed topology is illustrated in Fig. 2. It shows the block diagram of a CT-DSM with digital ELD compensation and a truncator. The exterior feedback path (Path 1) with one clock cycle delay compensates the half cycle ELD in the main feedback path. The block diagram of the DSM truncator is depicted at the top right of the Figure. The least significant bit to be removed is delayed by one cycle, and fed back to the truncator input. This results in a first-order noise shaping. Both Path 1 of the ELD compensation and Path 2 in the truncator have a one-cycle delay, and both are connected between the internal quantiser output and the truncator output. Hence, they can be combined.

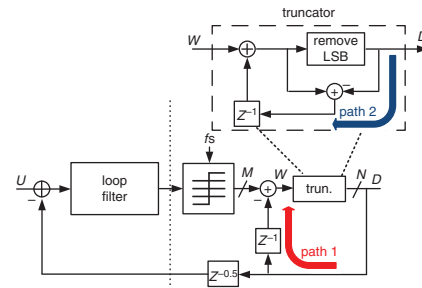


Fig. 2 Merging ELD compensation path and truncation feedback path

Fig. 3a shows the resulting fully digital implementation. After combining the two paths, a coefficient 2 results from the truncated output to the input of the internal quantiser. In a fully digital implementation, the topology has the same drawbacks as the structure described in [3]. The number of levels of the internal quantiser increases, which complicates the truncator implementation. Furthermore, the digital adder introduces an extra delay. Therefore, a better implementation is to perform the summation by shifting the reference levels of the internal quantiser as shown in Fig. 3b [1]. Then no extra quantiser levels are needed, and the digital adder is eliminated.

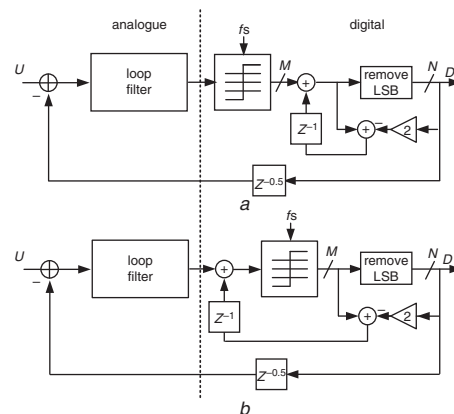


Fig. 3 Proposed topology with combined ELD and truncator

a With fully digital implementation
b With reference level shifting

Implementation: As an example, we consider a DSM with a 3-bit internal quantiser, and truncation to use a 2-bit DAC. Without truncation, the reference voltages are shifted to implement ELD compensation according to the block diagram in Fig. 4. By choosing the coefficient of the compensation path equal to 1, the shifted reference is simply the negative value of the digital output.

Fig. 5 shows the details of the digital ELD compensation with an embedded truncator. In Table 1, the entries of the reference shifting are the same as with only ELD compensation. The only difference is their order. Compared to digital ELD compensation using reference shifting [1], no extra circuit is needed here to control the shifting. The truncated output (D) and reference shifting values (Y) for the internal

quantiser outputs X are listed in the Table. Also, as the shift of the references is predetermined, only the routing needs to be changed in the circuit implementation to achieve the re-ordering.

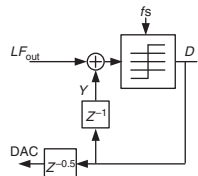


Fig. 4 Reference shifting with digital ELD compensation path, $Y = -D$

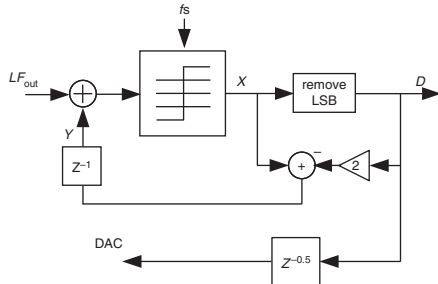


Fig. 5 Reference shifting, with ELD compensation path and truncator feedback path combined

Table 1: Reference shifting values with ELD compensation and truncator

| Output (X) | After truncation (D) | Reference shifting (Y) |
|----------------|--------------------------|----------------------------|
| 0 | 0 | -1 |
| 1 | 0 | 0 |
| 2 | 2 | -3 |
| 3 | 2 | -2 |
| 4 | 4 | -5 |
| 5 | 4 | -4 |
| 6 | 6 | -7 |
| 7 | 6 | -6 |

During truncation, the thermometer output code need not be converted into binary code. Instead, a simple encoder is required to convert the 8-level internal quantiser output into the 4-level final output and to control the DAC. Fig. 6 shows the digital circuit realising the conversion. Hence, the only extra loop delay is the delay of an OR gate. The output of each OR gate directly controls one DAC unit.

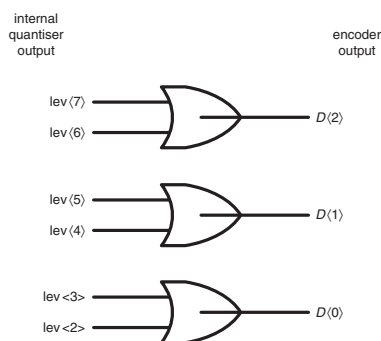


Fig. 6 Digital circuit truncating eight levels to four levels

Simulation results: A continuous-time $\Delta\Sigma$ modulator with the proposed ELD/truncation stage was simulated using macro-models. A 25 MHz bandwidth CT-DSM with a fourth-order loop filter and an out-of-band noise gain of 1.8 was designed assuming a 1.25 GHz sampling rate. The internal quantiser had eight levels, and its output was truncated into four levels. The output spectra with and without the truncator are shown in Fig. 7. Both spectra show an 83 dB signal-to-noise and

distortion ratio (SNDR), which verifies the effectiveness of the digital DSM truncator. Due to the digital truncation, the NTF at high frequencies is increased.

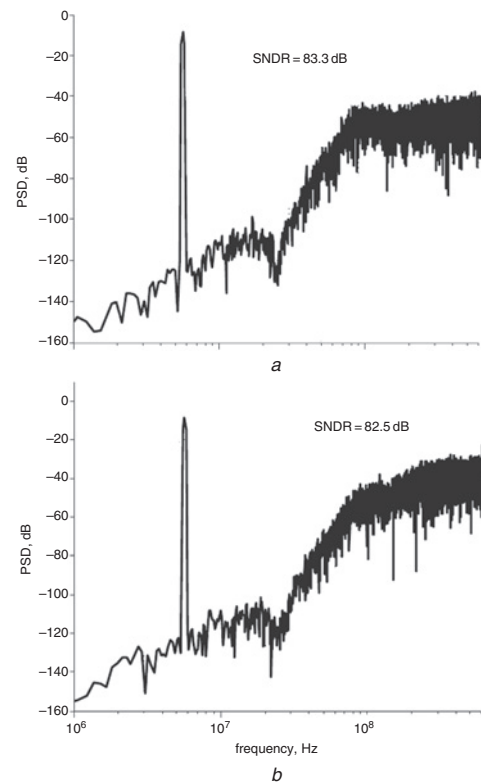


Fig. 7 Power spectra of DSM with ELD compensation

a Without truncation
b With truncation

Conclusion: In this Letter, a novel topology of a CT-DSM is proposed. The proposed architecture combines a digital DSM truncator with the digital ELD compensation circuitry. The truncator is implemented by sharing the digital ELD path and re-ordering the reference level shifting in the internal quantiser. The proposed topology only slightly increases the ELD, and may greatly simplify the DAC. Hence, it is suitable for high-speed implementation. Macro-model level simulations verified the effectiveness of the proposed topology.

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Submitted: 18 May 2015 E-first: 17 November 2015

doi: 10.1049/el.2015.1595

One or more of the Figures in this Letter are available in colour online.

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