AN ABSTRACT OF THE DISSERTATION OF

Napong Panitantum for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on June 13, 2011.

Title: Ultra-Low-Energy Transmitters for Battery-Free Wireless Sensor Networks.

Abstract approved:

_____

Terri S. Fiez Kartikeya Mayaram

As the number of autonomous data collection applications keep increasing, the demand for wireless sensor networks (WSNs) has seen explosive growth. In this dissertation, an ultra-low-energy WSN transmitter is developed to reduce the energy consumption of sensor nodes in WSNs. With an ultra-low-energy transceiver, it is possible to eliminate the battery in the sensor node and power itself with an energy harvester, thus creating a battery-free sensor node. A variety of applications can be accommodated with the battery-free sensor node as it has small size, light weight, and endless lifetime.

Two prototype WSN transmitters are implemented to demonstrate the transmitter energy minimization. The first transmitter incorporates a fast frequency calibration to shorten the oscillation frequency tuning time. This minimizes energy wasted during the transmitter start-up period. The energy consumption of the second transmitter that employs a power oscillator architecture is minimized by maximizing the

transmitter efficiency. The efficiency of the power oscillator circuit is analyzed and the design procedure for maximum efficiency is then developed.

Prototype WSN transmitters were fabricated in 0.18-μm CMOS technology. The first transmitter operates in the 915-MHz ISM band. With 0.5-MHz reference frequency, the transmitter takes only 72 μs for the BFSK frequency calibration. It dissipates a power of 1.91 mW while radiating a power of -2.9 dBm. The second transmitter operates in the 2.45-GHz ISM band on a single supply of 0.65 V. The transmitter has efficiency as high as 23 % at -5.2 dBm radiated power. This corresponds to a low power consumption of 1.34 mW.

©Copyright by Napong Panitantum
June 13, 2011
All Rights Reserved

Ultra-Low-Energy Transmitters for Battery-Free Wireless Sensor Networks

by
Napong Panitantum

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented June 13, 2011
Commencement June 2012

Doctor of Philosophy dissertation of Napong Panitantum presented on June 13, 2011

APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

Co-Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Napong Panitantum, Author

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincere gratitude to my advisors, Dr. Terri Fiez and Dr. Kartikeya Mayaram, for giving me an opportunity to be a part of their research group. Without their supports, advices, and reviews, I would not have completed my dissertation up to this degree of achievement. I would also like to extend my sincere thanks to The National Science Foundation (EF-0529223 and DBI-0454822) for providing financial support during my research.

I would like to thank James Ayers for his discussions and assistances on my work. I would also like to thank Thomas Brown, Triet Le, Robert Batten, Adam Heiberg, Steve Meliza, Chris Lindsley, Farhad Farahbakhshian, Hector Oporta, Vikrant Arumugam, Saeed Pourbagheri, Samira Zali Asl, Mohsen Nasroullahi, Ronghua Ni, Saurabh Saxena, Ankur Guha Roy, Chao Shi, Justin Goins, and other people in the analog/mixed-signal group for their friendships and many years of my experience.

I would like to thank all Thai friends at Oregon State University during these years for making my time in Corvallis enjoyable and memorable, and my friends in Thailand for keeping in touch throughout this long period.

Most importantly, I would like to express my deepest gratitude and love to my parents, my brothers, and my relatives, who always stand by me and support me since the first day of my life.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

ULTRA-LOW-ENERGY TRANSMITTERS FOR BATTERY-FREE WIRELESS SENSOR NETWORKS

1. INTRODUCTION

1.1 Wireless Sensor Networks in the Information Age

We live in the information age, a time when vast amounts of knowledge can be accessed at the click of a mouse. The primary source of instant information is the internet, a worldwide web of networks that has been rapidly developing since the early 1990s [1]. Today, internet users can access and share information from their laptops, cell phones, and other mobile devices at locations across the globe, making it easier than ever to stay connected. Because being online is now easier than ever, a constant flow of information from the internet and other electronic resources has come to shape our everyday lives: we listen to traffic radio to determine the quickest travel route, we use cell phones to check the weather forecast, and we rely on computers to keep track of warehouse inventory and order new supplies. Moving into the future, technology will continue to develop and spread across the globe, changing the way information is accessed and utilized.

But before information, from the internet or elsewhere, can be accessed and utilized, data must first be gathered and processed, as all meaningful information is assembled from bits of raw data. For example, before forecasters predict the weather, they collect raw data about temperature, humidity, barometric pressure, and wind speed. Forecasters then analyze this data and interpret it into a weather forecast, a

piece of meaningful information. In the past, data was collected, analyzed, and interpreted manually by humans. This process was slow, inefficient, and prone to errors. As a result, wireless sensor networks (WSNs) were introduced in the early 2000s [2]. Essentially, WSNs use sensor nodes to gather data, which is then sent to a central processing hub. The hub analyzes the data from the sensor nodes and interprets it into meaningful information, providing valuable feedback that can be accessed and utilized by a variety of users. In the future, WSNs will provide feedback to autonomous systems that can regulate themselves based on a set of specific conditions, laying the groundwork for a faster, more connected information age.

1.2 Overview of Wireless Sensor Networks

A WSN generally consists of multiple sensor nodes and a single processing hub distributed over an area of interest. As mentioned in Section 1.1, sensor nodes are input terminals that collect raw data. The data collected by each sensor node varies depending on its specific purpose, but all sensor nodes detect the physical conditions of their surroundings.

After sensor nodes collect raw data from their physical surroundings, they send that data to a dedicated node or central hub. Each sensor node in this application typically has a wireless communication distance of 5-40 meters. If one node wants to communicate with other nodes lying outside its boundary, it will use sensor nodes located along the line between itself and its destination as intermediate repeaters to

pass the data, as shown in Figure 1.1. With this peer-to-peer communication scheme, data can be transmitted over large distances, making a WSN's area of interest highly scalable—it could be as small as a building or as large as a city, depending on the number of sensor nodes.

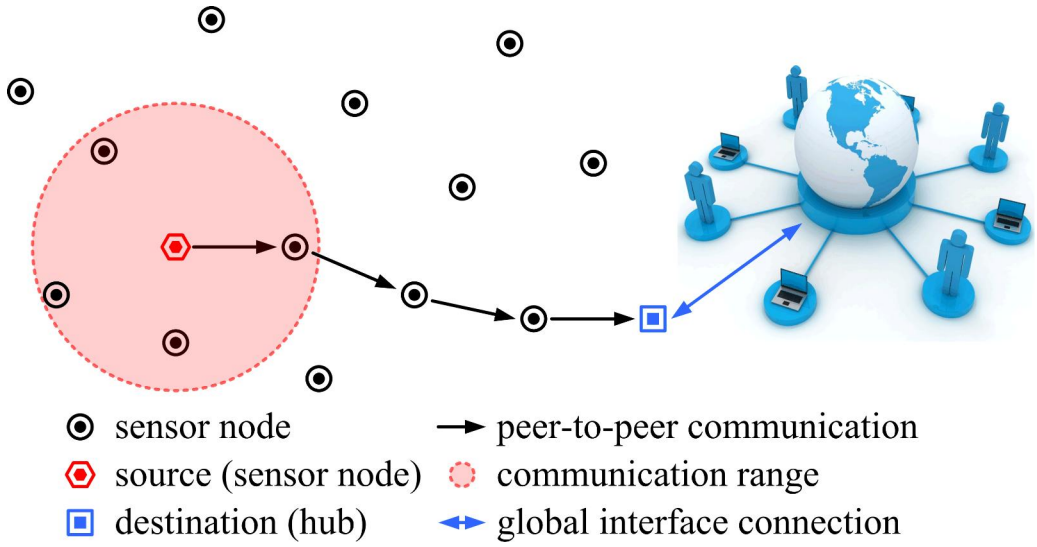

Figure 1.1. Conceptual communication topology of wireless sensor networks.

In short, WSNs are extremely flexible because they can process different types of information and accommodate different parameters of scale. As a result, WSNs have the potential to serve a range of purposes, from verifying a person's identification to regulating a city's sprinklers. However, few applications currently benefit from WSNs, as sensor nodes are generally too large, too heavy, and too short-lived to be of use. In order to make WSNs more useful and ubiquitous, new technologies must be developed to make them smaller, lighter, and longer-lasting.

1.3 Battery-Free Wireless Sensor Networks

Each sensor node of a WSN is made up of four basic parts: (1) a sensor interface (the actual sensor may be either integrated or external), (2) a power supply with power conditioning circuitry, (3) a digital controller with data memory, and (4) a wireless interface. Figure 1.2 shows four state-of-the-art sensor nodes that are commercially available today [3]-[4]. The specifications of these sensor nodes are summarized in Table 1.1. As seen in the table, the battery is the largest and heaviest part of these four sensor nodes. The operating lifetime of each sensor node is also defined by its battery, since the battery is the only energy source. As noted in Section 1.2, the key to improving the functionality of WSNs is developing new technologies that make sensor nodes smaller, lighter, and longer-lasting. For this reason, it is crucial to create a sensor node with a smaller battery and a longer lifespan. This will decrease the size and weight of sensor nodes while simultaneously maximizing their operating lifetime, thus making them more practical and efficient.

To overcome the problems presented by sensor node batteries, future WSNs will have energy harvesters. The energy supply for a WSN can be harvested from sunlight, thermal heat, vibration, radio frequency (RF) radiation, or a combination of these, depending on the environment where it is deployed [5]-[6]. An energy harvester will increase the lifetime of a WSN by acting as an additional power source for the sensor node. In addition, if a sensor node consumes extremely low amounts of energy, it will be able to operate solely on the power from an energy harvester. In this case, the energy harvester will collect the harvested energy and store it

temporarily, for example in a super capacitor, while the sensor node is inactive. Sensor nodes will then operate for a short period of time by using the stored energy. In this way, traditional WSNs will evolve into battery-free WSNs.

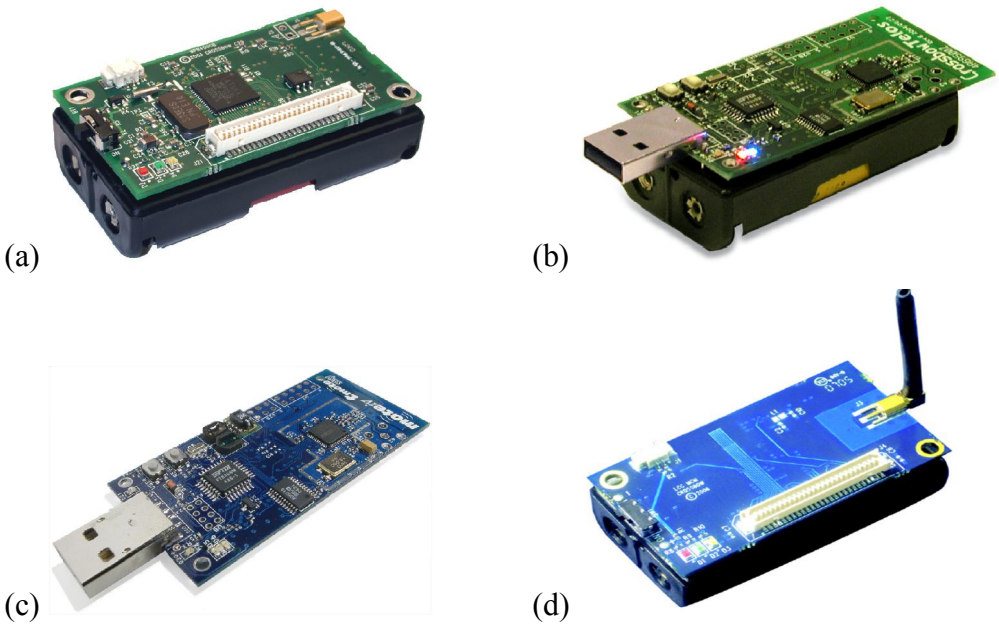

Figure 1.2. Commercial-off-the-shelf wireless sensor nodes. (a) MICA2, (b) TelosB, (c) Tmote Sky, and (d) IRIS.

Battery-free WSNs offer a number of advantages. First, eliminating a sensor node's battery reduces its size and weight; this could lead to sensor nodes being invisibly embedded in many objects, including walls, light fixtures, and appliances. In addition, a battery-free WSN has a virtually infinite lifetime; this would increase the lifespan of WSNs and eliminate the maintenance cost of replacing batteries.

Table 1.1. Summary of specifications of wireless sensor nodes in Figure 1.2.

Sensor node	MICA2	TelosB	Tmote Sky	IRIS
Carrier frequency	915 MHz	2.45 GHz	2.45 GHz	2.45 GHz
Data rate	38.4 kbps	250 kbps	250 kbps	250 kbps
Nominal supply	3 V	3 V	3 V	3 V
WSN receiver • Current • Sensitivity	 10 mA -98 dBm	 23 mA -94 dBm	 22 mA -94 dBm	 16 mA -101 dBm
WSN transmitter • Current • Radiation	 27 mA 5 dBm	 - 0 dBm	 20 mA 0 dBm	 17 mA 3 dBm
WSN controller • Active • Sleep	 8 mA 15 μA	 1.8 mA 5 μA	 1.8 mA 5 μA	 8 mA 8 μA
WSN form factor[1] • Dimensions • Weight	 58x32x7 mm 18 g	 65x31x6 mm 23 g	 65x32x7 mm -	 58x32x7 mm 18 g
2xAA batteries • Dimensions • Weight	2x14(diameter)x50(height) mm 2x23 g			
WSN lifetime[2]	1.0 year	1.1 year	1.2 year	1.1 year

[1]Excludes sensors and batteries.
[2]Assumed 2xAA 2400 mAh alkaline batteries and 1% duty cycle for peer-to-peer communication.

The key to creating battery-free WSNs is designing sensor nodes that consume ultra-low amounts of energy. According to Table 1.1, most of a sensor node's energy is consumed by its transceiver, which enables WSNs to communicate wirelessly. Thus, lowering the energy dissipation of transceivers is crucial to creating battery-

free WSNs. While techniques for reducing the energy consumption of WSN receivers have been discussed in [7]-[14], the research in this dissertation focuses on decreasing the energy consumption of WSN transmitters.

1.4 Dissertation Organization

This dissertation presents the architecture of an ultra-low-energy transmitter for battery-free WSNs. Chapter 2 discusses various transmitter parameters which are directly related to the transmitter energy consumption, including start-up time and transmitter efficiency. This chapter also reviews WSN communication systems, WSN transmitter architectures, and recently published WSN transmitters. The WSN transmitter designed to reduce start-up time by using a fast frequency calibration is outlined in Chapter 3. Chapter 4 provides the efficiency analysis and the design methodology for a high efficiency transmitter. The prototype WSN transmitter is presented along with measurement results. The conclusions of this dissertation are given in Chapter 5.

2. A DESIGN REVIEW OF ULTRA-LOW-ENERGY TRANSMITTERS FOR WIRELESS SENSOR NETWORKS

2.1 Introduction

In recent years, numerous applications employ wireless sensor networks (WSNs) to collect, transmit, and process data. As mentioned in Section 1.2, WSNs are extremely flexible in function and scale. For this reason, WSNs can be designed to perform any number of tasks, from controlling the temperature of an office building to checking the time on a parking meter.

Despite the fact that WSNs serve a wide range of purposes, all WSNs share several commonalities. For example, every WSN's area of operation is occupied by a series of sensor nodes. Since the wireless communication distance of each sensor node is typically limited to 5-40 meters, WSNs use a peer-to-peer communication scheme to transmit data over large distances. As a result, WSNs can consist of countless sensor nodes. In order to be compatible with all WSN applications, each sensor node must be essentially small, light, and energy efficient.

The key to reducing a sensor node's size and weight while increasing its efficiency is minimizing its energy consumption, as discussed in Section 1.3. If a sensor node runs solely on the power from its energy harvester, then its battery—which is usually the largest and heaviest part—can be eliminated, resulting in a lighter, smaller, and more efficient sensor node. The key parts of the sensor node that consume energy include the transmitter, receiver, and controller. This work focuses on the highest power consuming block: the transmitter. The transmitter generates the

radio frequency to wirelessly carry the data to another sensor node receiver. Thus, decreasing the energy consumption of a sensor node transmitter is crucial to improving its overall efficiency.

This chapter reviews design parameters associated with the energy consumption of WSN transmitters. It also discusses communication systems and transmitter architectures for ultra-low-energy transmitters. Finally, the performance parameters of recently published WSN transmitters are summarized.

2.2 Minimizing the Energy Consumption of WSN Transmitters

Figure 2.1 shows a simple block diagram of a generic wireless transmitter. This representation is composed of five blocks: (1) a radio frequency (RF) source, (2) a RF modulator, (3) a power amplifier (PA), (4) an impedance transformer, and (5) an antenna. The RF source generates the carrier signal, which is modulated by the baseband data. The power amplifier then amplifies the modulated signal before delivering it to the antenna through the impedance transformer.

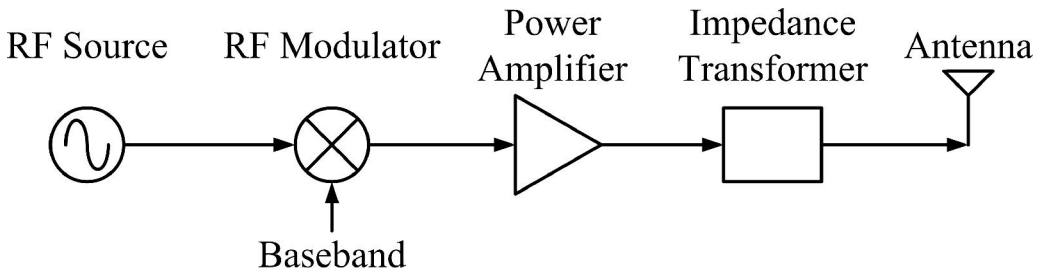

Figure 2.1. Generalized transmitter block diagram.

The energy consumption of the transmitter (E_{TX}) is expressed by:

$$E_{TX} = P_{start-up} t_{start-up} + P_{transmit} t_{transmit} \tag{2.1}$$

where $P_{start\text{-}up}$ and $t_{start\text{-}up}$ are the power consumption and the time duration of the start-up period before data transmission, respectively, and $P_{transmit}$ and $t_{transmit}$ are the power consumption and the time duration during data transmission. $P_{transmit}$ is comprised of the overhead power ($P_{overhead}$), a fixed amount of power consumption normally from the RF source and the RF modulator, and the power consumption of the power amplifier (P_{PA}). P_{PA} is equal to the radiated power (P_{rad}) at the antenna divided by the power amplifier efficiency (η_{PA}). $t_{transmit}$ is defined as the ratio of the number of bits (N_{bit}) and the bit rate (R_{bit}). Then E_{TX} can be rewritten as:

$$E_{TX} = P_{start-up} t_{start-up} + \left(P_{overhead} + \frac{P_{rad}}{\eta_{PA}} \right) \frac{N_{bit}}{R_{bit}}. \tag{2.2}$$

Note that this expression assumes that the impedance transformer is lossless. For a lossy impedance transformer, the loss can be modeled as a reduction in the efficiency of the power amplifier.

The energy consumption in long distance communication systems such as a cellular network is dominated by the high radiated power, which can be up to 30 dBm, and the large number of bits per transmission. As such, the energy consumed due to the overhead power and the start-up time is relatively insignificant. Therefore, minimizing the energy consumption for long distance communication systems depends solely on improving the efficiency of the power amplifier. However, for WSNs, the radiated power is typically less than 0 dBm because sensor nodes communicate over relatively short distances. In addition, the number of bits per

transmission is low, only from a few hundred to a thousand bits, due to the nature of WSN applications. As a result, all parameters in (2.2) become equally significant and must be accounted for in minimizing the energy consumption. Next, each parameter is examined individually.

A. Number of bits (N_{bit})

The energy consumption of transmitters can be minimized by shortening the transmission time between sensor nodes. In order to shorten the transmission time, the quantity of transmitted data must be reduced. This reduction is commonly performed by data compression algorithms in exchange for more computational power for compression and decompression at the source and destination sensor nodes. For typical WSN applications, simple algorithms, such as a run-length encoding or a delta encoding, offer a good compromise between reduced transmitted power and increased computational power. The benefits of data compression increase dramatically in a peer-to-peer communication scheme, where multiple nodes relay the same data. The relay sensor nodes save their energy without using any extra power for computation. The number of bits is generally in the range of 200 -1,000 bits ($N_{bit} \sim$ 200-1000).

B. Bit rate (R_{bit})

Increasing the bit rate can also reduce transmission time and thus minimize the transmitter energy consumption. However, the bit rate of WSNs is usually not limited by the WSN transmitter. Instead, the bit rate is typically defined by the WSN

receiver as it directly affects the receiver performance. A WSN receiver that has a higher bit rate generally has lower sensitivity and consumes higher power. The bit rate of state-of-the-art WSN receivers is in the range of 100 kbps-1 Mbps (R_{bit} ~ 100 kbps-1 Mbps).

C. Radiated power (P_{rad})

To minimize the transmitter energy consumption, the transmitter must radiate just enough power to reach the receiver within its communication distance. If the radiated power is too low, the communication fails. On the other hand, if the radiated power is too high, then energy is wasted. The radiated power is determined by two parameters: the sensitivity of the receiver and the attenuation over the communication distance or the path loss. Details of these two parameters are given in Section 2.3 where the WSN communication system is discussed. The radiated power for a short communication distance is usually below 0 dBm (P_{rad} < 0 dBm).

D. Start-up power ($P_{start\text{-}up}$)

The start-up power is the power that the transmitter dissipates during the start-up phase. The transmitter consumes this power while waiting for the RF source and the RF modulator to settle. In long distance communication systems where each transmitter block is completely isolated from the others, the start-up power is normally reduced to just equal the overhead power by disabling the power amplifier. This substantially decreases the start-up power because the power amplifier consumes much higher power than the other transmitter blocks. In WSNs, however,

all transmitter blocks are designed together in order to minimize the energy consumption. Disabling the power amplifier is thus not possible since it will disturb the RF source and the RF modulator. As a result, the start-up power in this case is approximately the same as the power consumption during the data transmission ($P_{start\text{-}up} \approx P_{transmit}$).

E. Start-up time ($t_{start\text{-}up}$)

The start-up time is defined as the time period after the transmitter is powered on until it is ready to send data to the receiver. This period is typically required for the RF source and the RF modulator to settle to their operating points. If the transmission time is fairly long, the energy wasted during the start-up time will be negligible. However, the transmission time of WSNs is relatively short as only a small number of bits are transmitted in one single communication. Thus, the energy wasted during this time becomes more significant. For example, assume N_{bit} = 500 bits and R_{bit} = 250 kbps, then $t_{transmit}$ = 2 ms. If $t_{start\text{-}up}$ = 1 ms, the start-up energy consumption when $P_{start\text{-}up} \approx P_{transmit}$ is approximately 50 % of the energy consumption during the data transmission or 33 % of the total transmitter energy consumption. The percentage of energy wasted is increased for WSNs that employ a lower number of bits and/or a higher bit rate. For this reason, the start-up time of WSNs must be reduced in order to minimize the transmitter energy consumption.

F. Overhead power ($P_{overhead}$) and power amplifier efficiency (η_{PA})

The last two parameters in (2.2) are the overhead power and the power amplifier efficiency. These two parameters can be represented by a single parameter as the transmitter efficiency (η_{TX}), which is expressed as:

$$\eta_{TX} = \frac{P_{rad}}{P_{overhead} + \frac{P_{rad}}{\eta_{PA}}}. \tag{2.3}$$

The transmitter efficiency indicates how effectively the transmitter converts the power consumed into the radiated power. A higher transmitter efficiency implies that the transmitter consumes lower power and, hence, lower energy for the same radiated power. To improve the transmitter efficiency, the overhead power must be minimized and the power amplifier efficiency must be maximized.

The maximum transmitter efficiency depends largely on the level of the radiated power. When the radiated power is high ($P_{overhead} << P_{rad}/\eta_{PA}$), the maximum transmitter efficiency is limited by the power amplifier efficiency. Conversely, when the radiated power is low ($P_{overhead} >> P_{rad}/\eta_{PA}$), the maximum transmitter efficiency is limited by the ratio of the radiated and overhead power. Since the peer-to-peer communication scheme of WSNs requires only a small amount of radiated power, WSN transmitters therefore must be designed to minimize the overhead power. Subsequently, the power amplifier efficiency must be maximized.

While there are various parameters for minimizing the transmitter energy consumption, the number of bits, bit rate, and radiated power are defined by the system level of WSN communication. This work focuses on the circuit level where

the transmitter start-up time will be minimized and the transmitter efficiency will be maximized.

2.3 WSN Communication Systems

There are two types of communication schemes for implementing wireless transceivers: narrowband communication and ultra-wideband (UWB) communication. Narrowband communication is a traditional system where data is modulated onto a continuous wave or a carrier. The power spectral density of this wave is concentrated in a narrow bandwidth of a few tens of kHz to MHz. In a UWB communication system, data is modulated onto a series of pulses and the pulse power is spread over a large bandwidth. These two communication systems are compared with each other in order to determine the one that is preferred for battery-free WSN applications.

The comparison uses the communication distance as the criterion for selecting the communication scheme. First, the maximum radiated power of the transmitter is determined. Receiver sensitivity data from a variety of published WSN receivers is then reported. The ratio of the maximum radiated power to the receiver sensitivity indicates the maximum attenuation that the transmitted data can withstand. This maximum attenuation is converted into a communication distance through a path loss model.

A. Maximum radiated power

The maximum radiated power is established to ensure that one communication channel does not corrupt a nearby communication channel. The restriction on the radiated power usually varies from country to country. In the United States, the restriction is written by the Federal Communications Commission (FCC) in Title 47 of the Code of Federal Regulations Part 15 [15].

The FCC specifies different maximum powers for different narrowband applications and frequencies. However, only the industrial, scientific, and medical (ISM) bands are considered here since ISM bands allow unlicensed communications. Out of the 11 ISM bands, the 915-MHz and 2.45-GHz bands are two bands that provide a good compromise between a compact antenna with efficient transmission and a moderate penetration on various terrains [16]. The maximum radiated power for these two narrowband bands is 30 dBm (1 W).

For the UWB communication system, the FCC does not have any specific number on the maximum power. Instead, the power transmission of the UWB system is restricted through a power spectral density mask. Figure 2.2 shows the mask for indoor UWB systems. The maximum radiated power is calculated by integrating the area under the entire mask. However, this integrated power is unrealistic as there is no real pulse that can exactly fit into the corners of the rectangular mask. The realizable pulse that can occupy most of the mask is the 5^{th} order derivative Gaussian pulse [17]. The calculated maximum radiated power of this Gaussian pulse is -5.4 dBm. There are typically losses of a few dB to allow for margin and, hence, the

practical maximum radiated power of the UWB communication system is approximately -8 dBm.

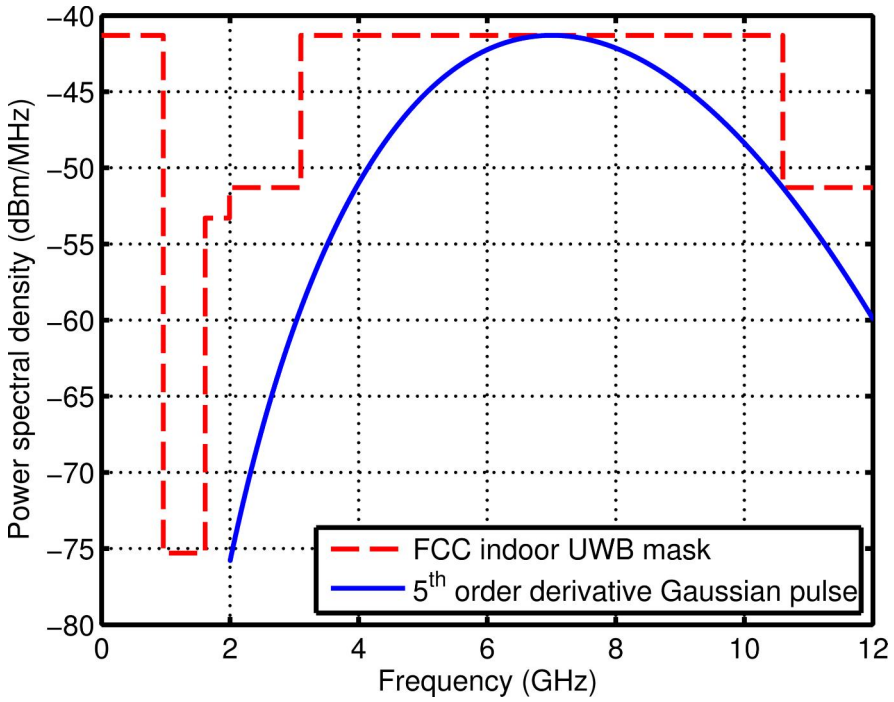

Figure 2.2. The FCC power spectral density mask for indoor UWB systems and the power spectral density of the 5th order derivative Gaussian pulse.

B. Receiver sensitivity

Communication between sensor nodes succeeds when the data is successfully transferred from a transmitter to a receiver. The receiver, therefore, is as important as the transmitter for determining the performance of the communication link. Key performance metrics of recently published state-of-the-art WSN receivers, both narrowband and UWB communication systems, are summarized in Table 2.1 and Table 2.2, respectively. Classified by architecture, narrowband receivers can be divided into four types: (1) frequency down-conversion [7]-[8], (2) envelope

detection [9], (3) wake-up [10]-[11], and (4) super regeneration [12]-[14]. UWB receivers can be categorized into two types: (1) frequency down-conversion [18]-[20], and (2) energy detection [21]-[22].

Table 2.1. Performance summary of recently published narrowband WSN receivers.

	Tech.	Frequency	Power	Data Rate	Energy	Sensitivity
[7]	0.25 μm	915 MHz	800 μW	20 kbps	40 nJ/b	-90 dBm
[8]	0.13 μm	2.45 GHz	330 μW	300 kbps	1.1 nJ/b	-
[9]	0.18 μm	915 MHz	2.6 mW	1 Mbps	2.6 nJ/b	-65 dBm
[10]	90 nm	2.0 GHz	52 μW	100 kbps	520 pJ/b	-72 dBm
[11]	65 nm	2.45 GHz	415 μW	500 kbps	830 pJ/b	-82 dBm
[12]	0.13 μm	2.45 GHz	2.8 mW	500 kbps	5.6 nJ/b	-90 dBm
[13]	90 nm	403 MHz	400 μW	120 kbps	3.3 nJ/b	-93 dBm
[14]	0.18 μm	2.45 GHz	215 μW	2 Mbps	175 pJ/b	-75 dBm

Table 2.2. Performance summary of recently published UWB WSN receivers.

	Tech.	Input BW	Pulse Rate	Energy	Sensitivity
[18]	0.18 μm	-	20 Mpps	1.44 nJ/p	-
[19]	0.18 μm	600 MHz	15.6 Mpps	6.5 nJ/p	-75 dBm
[20]	0.13 μm	1.5 GHz	15.6 Mpps	3.3 nJ/p	-79 dBm
[21]	90 nm	570 MHz	100 kpps	2.5 nJ/p	-99 dBm
[22]	0.13 μm	850 MHz	3.9 Mpps	1.1 nJ/p	-78 dBm

Narrowband receivers consume very little power and achieve energy efficiency on the order of nanojoule per bit (nJ/b) or lower. UWB receivers consume much

higher power than narrowband receivers but achieve comparable energy efficiency of a few nanojoules per pulse (nJ/p) due to a high pulse rate. Except for wake-up receivers, the average sensitivity of narrowband receivers scales from -80 dBm at 1 Mbps to -90 dBm at 100 kbps. The average sensitivity of UWB receivers scales from -78 dBm at 10 Mpps to -98 dBm at 100 kpps. These receiver sensitivities will be used as a reference to determine the communication distance of both narrowband and UWB communication systems.

C. Communication distance

The communication distance is the maximum distance over which a transmitter and a receiver are able to communicate. It depends on the ratio of the maximum radiated power of the transmitter and the sensitivity of the receiver. This ratio is the path loss which can be translated directly into the communication distance.

A simple equation for the path loss (PL) in dB is

$$PL = n \cdot 10 \cdot \log_{10}(d) + PL_0 \tag{2.4}$$

where n is an attenuation coefficient depending on the communication environment, d is the distance in meters, and PL_0 is the reference path loss at 1 meter in dB. Table 2.3 summarizes n and PL_0 for line-of-sight (LOS) and non-line-of-sight (NLOS) path losses in both narrowband (915-MHz and 2.45-GHz bands) [23] and indoor UWB [24] communications. The relationship between path loss and distance is plotted in Figure 2.3.

Table 2.3. Path loss parameters of narrowband (915-MHz and 2.45-GHz bands) and indoor UWB communications for LOS and NLOS environments.

Path loss parameter	915 MHz		2.45 GHz		UWB	
	LOS	NLOS	LOS	NLOS	LOS	NLOS
n	2.18	2.58	2.18	2.58	1.7	3.1
PL_0 (dB)	31.7		40.2		47.3	50.5

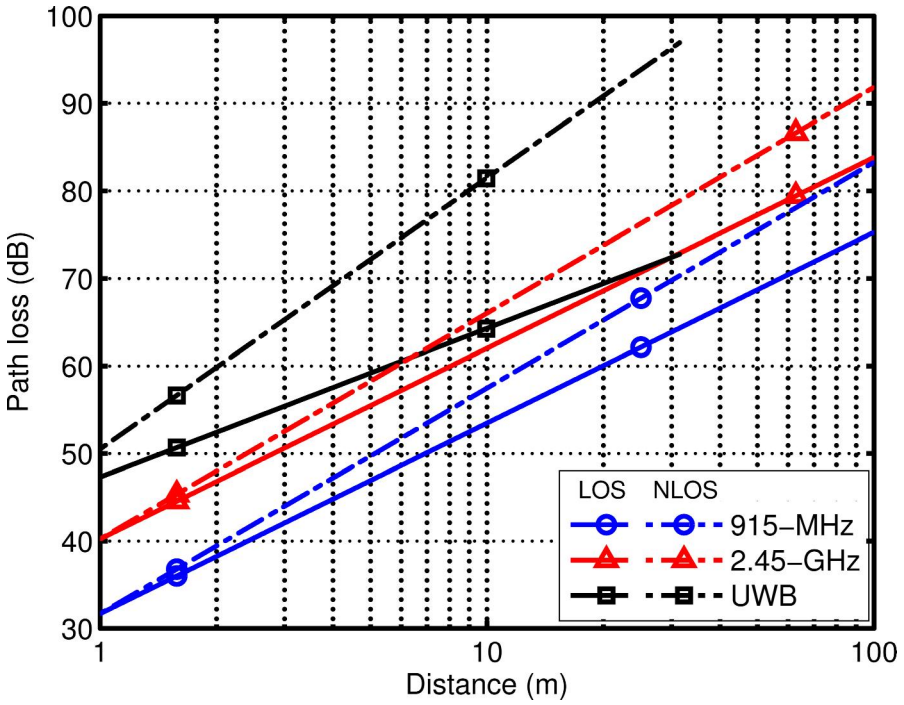

Figure 2.3. Path loss of narrowband (915-MHz and 2.45-GHz bands) and indoor UWB communications for LOS and NLOS environments.

Narrowband communication, which has a maximum radiated power of 30 dB and a receiver sensitivity of -80 dBm at 1 Mbps, can tolerate a path loss up to 110 dB. This is equivalent to a communication distance of hundreds of meters. The UWB communication distance can be determined similarly with a maximum radiated power of -8 dBm and a receiver sensitivity of -88 dBm at the same 1 Mbps.

However, a bandwidth scaling must be included. The Gaussian pulse in Figure 2.2 spreads its -8-dBm maximum radiated power over approximately 6-GHz bandwidth while the average input bandwidth of receivers in Table 2.2 is about only 1 GHz. To match these two bandwidths, the input bandwidth is scaled up by a factor of 6. The receiver sensitivity is generally increased up to 8 dB due to the increased received noise. Thus, the path loss of UWB communication is approximately 72 dB. This translates to the UWB communication distance of about 30 meters in LOS or less than 5 meters in NLOS.

This limited communication distance makes the UWB system impractical for WSNs where sensor nodes are separated by 10 meters or more. As a result, the narrowband communication system is preferred for implementing WSNs where communicating sensor nodes are 10-40 meters apart. Furthermore, with a separation distance limited to 10-40 meters, the narrowband transmitter does not need to output the 30-dBm maximum radiated power. It can still communicate effectively while decreasing its radiated power to a range of -10 to 0 dBm to minimize energy consumption as mentioned in Section 2.2. The architecture of narrowband transmitters for WSNs is outlined in the following section.

2.4 WSN Transmitter Architectures

In a narrowband communication system, the transmitter architecture can be divided into two categories: frequency up-conversion and direct modulation. Both

architectures are briefly reviewed before comparing the recent publications of WSN transmitters.

A. Frequency up-conversion architecture

Block diagrams of narrowband transmitters using the frequency up-conversion architecture are illustrated in Figure 2.4. First, the data is modulated in the digital domain using a digital modulator and then converted into the signal at the baseband frequency by a digital-to-analog converter (D/A). Later the baseband signal is up-converted to the RF frequency by a mixer. The RF signal is then amplified by a power amplifier (PA) before transmitting the output power to an antenna via a matching network (MN). The frequency up-conversion can further be categorized into two architectures: the heterodyne frequency up-conversion and the homodyne frequency up-conversion.

The heterodyne frequency up-conversion architecture, shown in Figure 2.4(a), employs two sets of mixers. The first mixer up-converts the baseband signal to the intermediate frequency (IF). The second mixer then up-converts the IF signal to the RF frequency. The second up-conversion creates an RF signal with two sidebands, and thus a bandpass filter (BPF) is required to reject the unwanted sideband after the second mixer. This architecture is very robust and is widely used in cellular phones particularly in the early generation phones. However, transmitters with the heterodyne frequency up-conversion architecture normally consume high levels of power, as they are comprised of many circuit blocks.

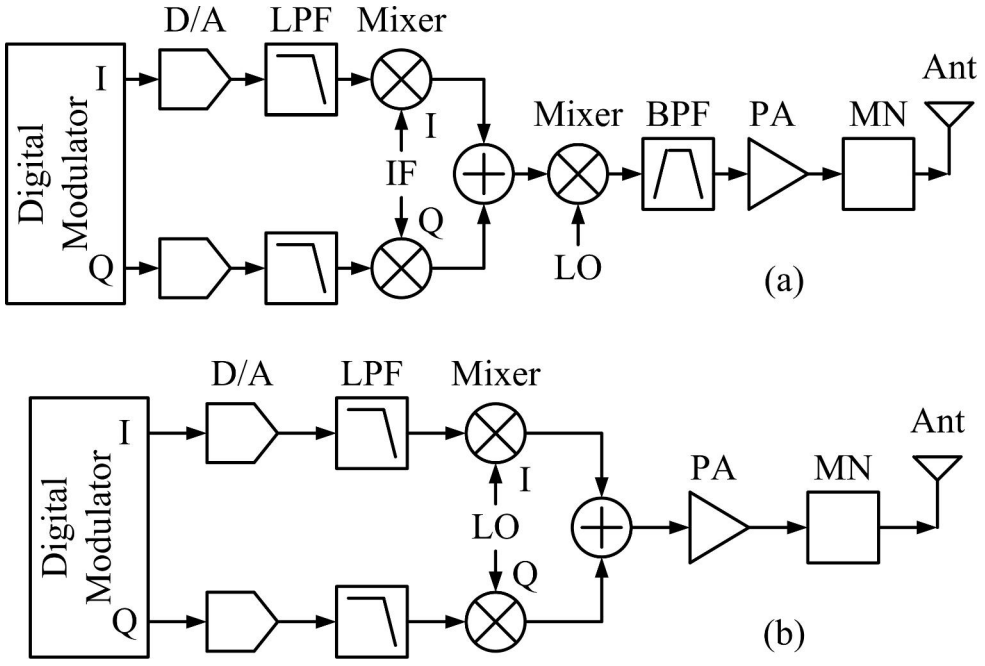

Figure 2.4. Block diagrams of transmitters using frequency up-conversion. (a) Heterodyne, and (b) homodyne architectures.

An alternative to the heterodyne frequency up-conversion architecture is the homodyne architecture depicted in Figure 2.4(b). Here, the baseband signal is directly up-converted to the RF signal. The power consumption of the homodyne architecture is generally lower than that of the heterodyne architecture due to the elimination of the second mixer and the bandpass filter. Thus, this architecture is more suitable for compact portable wireless communication devices. A drawback of the homodyne architecture is the pulling of the local oscillator (LO). With a single up-conversion, the LO and the RF frequencies are similar. The RF leakage, either by coupling from a power amplifier or by radiating from an antenna, can pull the LO

away from its desired oscillation frequency. The local oscillator, therefore, must be carefully designed to withstand the frequency pulling.

In addition, a quadrature structure is typically employed in the frequency up-conversion architecture in order to support high spectral efficiency modulation schemes such as QPSK, QAM, etc. The data is split into an in-phase (I) and quadrature (Q) components. Both in-phase and quadrature data are up-converted by their respective in-phase LO/IF and quadrature LO/IF. The quadrature structure is particularly useful in bandwidth-constrained communication systems since it decreases the required bandwidth by half for the same data rate or increases the data throughput to twice for the same bandwidth.

B. Direct modulation architecture

Figure 2.5 shows the block diagram of a direct modulation transmitter. As the name suggests, data is modulated to the RF frequency by directly changing the RF signal without the use of a mixer. The direct modulation architecture is simpler and consumes significantly less power than the frequency up-conversion architecture because it has a smaller number of circuit blocks. However, this architecture can support only a few simple modulation schemes.

The on-off keying (OOK) modulation, an extreme case of amplitude shift keying (ASK) modulation, is accomplished by turning either the power amplifier or the oscillator on and off. The transmitter also saves energy during the off period.

However, the data rate of this modulation scheme is limited by how fast the power amplifier or the oscillator can be turned on and off.

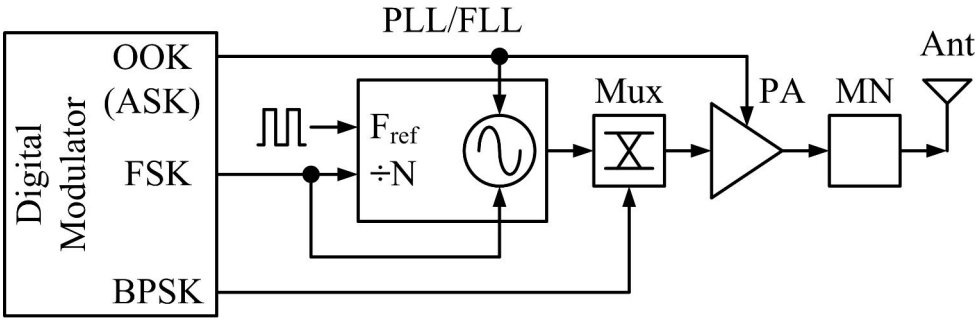

Figure 2.5. Block diagram of a transmitter using the direct modulation architecture.

Another popular modulation for this architecture is frequency shift keying (FSK). The RF frequency can be modulated in two ways. The first approach is changing the frequency divider ratio in a phase-locked loop (PLL) or frequency-locked loop (FLL). The PLL/FLL, as an RF source, generates the RF frequency by multiplying the frequency of a stable low-frequency reference such as a crystal oscillator. Thus, changing the frequency multiplication or divide ratio moves the RF frequency. In this approach the maximum data rate is set by the bandwidth of the PLL/FLL. The second approach is to directly change the frequency of the oscillator inside the PLL/FLL. In this case, the data rate is not tied to the PLL/FLL bandwidth. However, the oscillation frequency must be precisely tuned and stored for all FSK frequencies prior to the modulation.

The last possible modulation is phase shift keying (PSK). For a differential oscillator, binary PSK (BPSK) modulation is done by multiplexing the differential

outputs for a 180-degree phase shift. The abrupt change of phases in BPSK causes the spectrum to spread out into sidebands. Thus, BPSK modulation has less spectral efficiency than OOK or FSK modulations.

2.5 Recently Published WSN Transmitters

This section summarizes recently published state-of-the-art WSN transmitters. These transmitters are classified by their architecture described in the previous section. Table 2.4 shows key performance parameters of frequency up-conversion WSN transmitters while Table 2.5 presents the same parameters for direct modulation WSN transmitters.

Table 2.4. Performance summary of recently published frequency up-conversion WSN transmitters.

	Tech.	Frequency	Consumed power	Radiated power	Efficiency
Heterodyne frequency up-conversion					
[25][1]	0.25 μm	2.4 GHz	16 mW	0 dBm	6.25 %
[26]	0.18 μm	868 MHz	38.8 mW	9.5 dBm	23.0 %
[27]	0.13 μm	915 MHz	3.16 mW	-7.0 dBm	6.31 %
Homodyne frequency up-conversion					
[28]	0.5 μm	434 MHz	25 mW	9.8 dBm	38.0 %
[29][1]	0.18 μm	2.4 GHz	5.4 mW	0 dBm	18.5 %
[30]	0.18 μm	915 MHz	28.8 mW	0 dBm	3.47 %
[31]	0.18 μm	405 MHz	1.87 mW	-12 dBm	3.34 %
[32]	0.13 μm	915 MHz	2.7 mW	-6 dBm	9.26 %
[33][1]	90 nm	960 MHz	23.3 mW	10.3 dBm	46.0 %

[1]Without LO generation.

Table 2.5. Performance summary of recently published direct modulation WSN transmitters.

	Tech.	Frequency	Consumed power	Radiated power	Efficiency
Power amplifier OOK direct modulation					
[9]	0.18 μm	915 MHz	9.1 mW	-2.2 dBm	6.62 %
[34]	0.18 μm	2.4 GHz	11.2 mW	0 dBm	8.93 %
[35]	90 nm	2.4 GHz	3.88 mW	0 dBm	25.8 %
Oscillator OOK direct modulation					
[36]	-	1.9 GHz	1.65 mW	-4.2 dBm	23.0 %
[37]	0.13 μm	1.9 GHz	2.63 mW	0.8 dBm	45.7 %
[38]	0.13 μm	1.9 GHz	3.6 mW	0 dBm	27.8 %
[39]	0.18 μm	440 MHz	5.2 mW	-0.2 dBm	18.4 %
PLL/FLL divider FSK direct modulation					
[40]	0.25 μm	434 MHz	5.0 mW	0 dBm	20.0 %
[41]	0.18 μm	2.4 GHz	28.3 mW	3 dBm	7.08 %
Oscillator FSK direct modulation					
[7]	0.25 μm	915 MHz	1.3 mW	-6 dBm	19.2 %
[8]	0.13 μm	2.4 GHz	1.0 mW	-5.2 dBm	30.0 %
[42]	0.13 μm	5.2 GHz	4.25 mW	0 dBm	23.5 %
[43]	0.18 μm	915 MHz	0.7 mW	-10 dBm	14.3 %

In the frequency up-conversion transmitters listed in Table 2.4, heterodyne transmitters consume more power than homodyne transmitters for the same radiated power because of the extra circuit blocks as mentioned in Section 2.4. None of these frequency up-conversion transmitters with radiated power of 0 dBm or below (shaded in Table 2.4) has efficiency greater than 10 % (except [29] since LO

generation power is not included). These transmitters with a low radiated power have poor efficiency since they have a relatively high overhead power.

On the contrary, there is at least one direct modulation transmitter in each of the four categories listed in Table 2.5 that radiates power of 0 dBm or lower but still has efficiency of 20 % or higher (shaded in Table 2.5). The efficiency is substantially improved particularly at low radiated power because the direct modulation architecture has fewer circuit blocks and hence has lower overhead power than the frequency up-conversion architecture. Thus, in terms of low energy consumption, direct modulation is preferred for use in the WSN transmitter.

2.6 Battery-Free WSN Transmitters

Battery-free WSNs are ultra-low-energy WSNs where sensor nodes are powered by energy harvesters instead of batteries. By getting rid of batteries which are commonly used as the main power source in today's WSNs, sensor nodes will be more compact, lighter, and have virtually infinite lifetime. These improvements will allow battery-free WSNs to be applied to many new applications.

To make battery-free WSNs viable, the WSN transmitter must consume as little energy as possible. First, the WSN transmitter is designed to radiate in the range of -10 to 0 dBm. This is sufficient radiated power to communicate to WSN receivers within 10-40 meters. A direct modulation architecture is employed for low overhead power. To further minimize the energy consumption, the transmitter start-up time is shortened by using a fast frequency calibration described in Chapter 3. The direct

modulation transmitter with a high efficiency design is demonstrated in Chapter 4. The developed WSN transmitter in conjunction with OOK receivers in [9],[12]-[13] or FSK receivers in [7]-[8],[14] forms the basis for ultra-low-energy WSN transceivers for battery-free WSNs.

3. A 915-MHZ WSN TRANSMITTER WITH FAST FREQUENCY CALIBRATION

3.1 Introduction

As wireless sensor networks (WSNs) continue to become larger and more complex, it is essential that more efficient and reliable sensor nodes be designed. As discussed in Section 1.2, WSNs use a peer-to-peer communication scheme to transmit data over large distances. This makes the development of more energy-efficient sensor nodes especially important, since a WSN can consist of countless interconnected sensor nodes. As a result, it is crucial to minimize the energy consumption of sensor nodes without compromising their overall performance. The primary focus of minimizing the energy consumption here is on the WSN transmitter since it dissipates comparatively higher energy than other circuits in the sensor node.

In a conventional transmitter, data transmission is the operation that consumes the most energy. However, in WSN transmitters, energy consumption during data transmission is much lower because the transmission distance is shorter and the radiated power is lower. Generally, WSN data transmission periods are shorter because smaller amounts of data are transmitted between nodes. In addition, the radiated power is usually lower because communication distances tend to be shorter. This means that minimizing the energy wasted during a WSN transmitter's start-up period is crucial to improving a sensor node's energy-efficiency, as mentioned in Section 2.2.

Tuning the oscillator frequency is generally the longest operation during a transmitter's start-up. This chapter discusses fast frequency calibration, which shortens the time it takes to tune the oscillator, thus reducing the overall energy consumption of the sensor node transmitter. The fast frequency calibration technique is incorporated into a low-power 915-MHz transmitter as the prototype. It is designed to communicate with the low-power super-regenerative receiver presented in [44].

3.2 Fast Frequency Calibration

The primary requisite for all radio transmissions is to generate a radio frequency (RF) as a carrier signal. RF generation can be accomplished by a variety of oscillator topologies, including LC-based, relaxation, or ring oscillators. However, the oscillation frequency varies widely with process, voltage, and temperature variations. Therefore, frequency tuning is required to control the oscillation frequency. The only exception is an oscillator based on the RF MEMS resonator where the resonant frequency is well-defined by high-precision physical dimensions and has good frequency stability over a wide range of temperatures [45].

The most commonly used frequency tuning circuit is the phase-locked loop (PLL). A PLL is comprised of a frequency divider, phase-frequency detector (PFD), charge pump, loop filter, and voltage controlled oscillator (VCO), as shown in Figure 3.1(a). The frequency divider senses the frequency of the oscillation signal (F_{osc}) and divides it down by an integer number (N). The phase of the frequency-divided signal

($F_{osc/N}$) is then compared with the phase of the reference signal (F_{ref}) at the PFD. The phase difference is fed to a charge pump and loop filter and is finally converted into the control voltage for the oscillator. This feedback loop forces $F_{osc/N}$ and F_{ref} phases to be the same, hence their frequencies are equal. The frequency of F_{osc} is therefore N times the frequency of F_{ref}.

The shortcoming of using a PLL as the frequency tuning circuit is its long locking time. The PLL locking time is inversely proportional to the PLL loop bandwidth and the frequency accuracy. As a rule of thumb, the PLL loop bandwidth must be less than 10 times the reference frequency for the stability of the feedback loop. The locking time usually takes up to hundred cycles or more of F_{ref} for the oscillation frequency to settle within the accuracy of 1%. Therefore, the locking time of PLLs must be reduced in order to minimize the energy consumption of transmitters in WSNs.

Figure 3.1(b) displays the timing diagram of an example PLL. At t_1, the PLL is locked since the rising edges of $F_{osc/N}$ and F_{ref} are aligned. If the oscillation frequency is exactly N times the reference frequency, the rising edge of $F_{osc/N}$ is still aligned with that of F_{ref} at t_2. If the oscillation frequency is higher or lower than N times the reference frequency, the $F_{osc/N}$ rising edge then rises earlier or later, respectively, compared to the F_{ref} rising edge at t_2. In other words, the frequency divider can be used as the frequency discriminator at t_2 when $F_{osc/N}$ and F_{ref} phases start simultaneously at t_1.

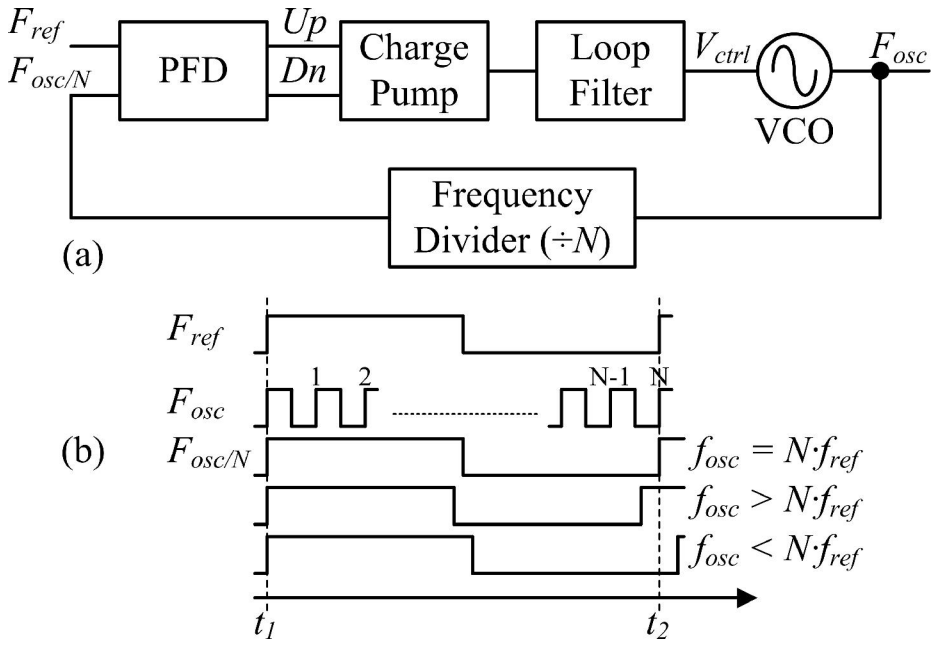

Figure 3.1. Phase-locked loop. (a) Block, and (b) timing diagrams.

By adding a reset signal (R_{div}) which forces the frequency divider at t_1 to be under the same condition as when these phases are aligned, the frequency calibration loop shown in Figure 3.2(a) is constructed. Both $F_{osc/N}$ and F_{ref} are evaluated using the rising-edge comparator to determine whether the oscillation frequency is higher or lower than N times the reference frequency. The calibration control takes the output from the rising-edge comparator and then adjusts the oscillation frequency until it equals N times the reference frequency.

Two additional periods, t_0-t_1 and t_2-t_3, depicted in Figure 3.2(b), have been added at the beginning and at the end of the frequency comparison period. Through t_0-t_1 the frequency divider gets reset while waiting for the oscillator frequency to stabilize after the calibration control output changes. The calibration control uses the t_2-t_3

period to evaluate the comparator output before adjusting the oscillation frequency for the next frequency comparison. Thus, only two cycles of F_{ref} are taken to run one frequency comparison. For the digitally controlled oscillator (DCO), the calibration control typically employs a successive approximation register (SAR) algorithm to calibrate the oscillation frequency. With an m-bit DCO, the entire frequency calibration will take m frequency comparisons and hence finish within $2 \cdot m$ cycles of F_{ref}.

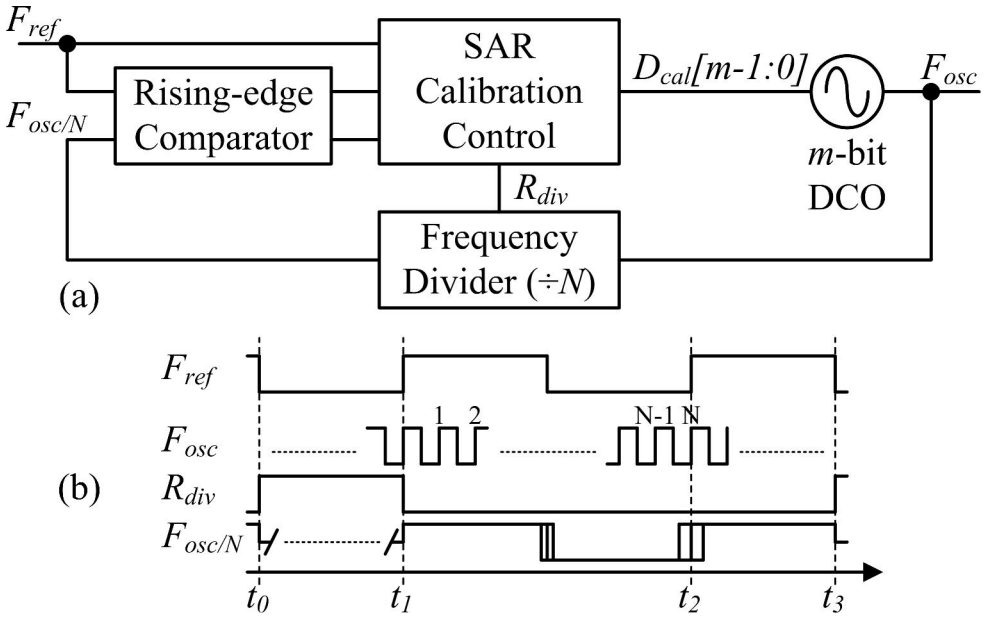

Figure 3.2. Fast frequency calibration loop. (a) Block, and (b) timing diagrams for a DCO with the SAR algorithm.

The advantages of this fast frequency calibration technique over the calibration technique in [46] are simplicity and higher energy efficiency. In [46], a charge pump is used to convert the difference of F_{ref} and $F_{osc/N}$ periods into a difference of voltages held on capacitors. The oscillation frequency is then adjusted based on this

voltage difference. Instead of using a reset signal such as the frequency calibration loop in Figure 3.2, the calibration technique in [46] holds voltages on capacitors, eliminating the need for phase alignment. Both frequency calibration techniques use two cycles of F_{ref} for one frequency comparison. Thus, the frequency calibration time of both techniques is the same for the same reference frequency. However, the technique of [46] requires a F_{ref} with 8 phases, a phase selector, a charge pump, and a voltage comparator. Therefore, it is more complicated and consumes more power than the frequency calibration technique proposed in Figure 3.2.

Despite the simplicity and low power consumption, the proposed fast frequency calibration technique has limited frequency accuracy. Even though R_{div} resets the frequency divider to the same condition as when the PLL is locked, it does not guarantee that F_{osc} rises exactly at t_1. For this reason, the initial phase of F_{osc} can be off by up to one cycle. As a result, the calibrated frequency can deviate systematically up to one-N^{th} of the oscillation frequency, which equals the frequency of F_{ref}. Thus, the F_{ref} frequency should be as high as tolerable frequency accuracy to minimize the frequency calibration time.

The fast frequency calibration technique can be used in many applications where low power consumption is important. This calibration technique can be used with wideband VCOs, which reduce phase noise by employing multiple sub-bands [46]-[48]. As long as two consecutive sub-bands overlap and are greater than the reference frequency, this frequency calibration technique will quickly search for the closest sub-band before allowing the VCO to operate normally. Figure 3.3 illustrates

the concept of this wideband VCO frequency tuning. By sharing the frequency divider for both loops, the implementation of this frequency tuning circuit is compact. The calibration technique is also ideal for ultra-low-energy WSN transmitters communicating to super-regenerative receivers with a wide input bandwidth. The wide input bandwidth helps accommodate the transmitter frequency variation due to the limited frequency accuracy. The circuit implementation of this fast frequency calibration technique is described in the next section.

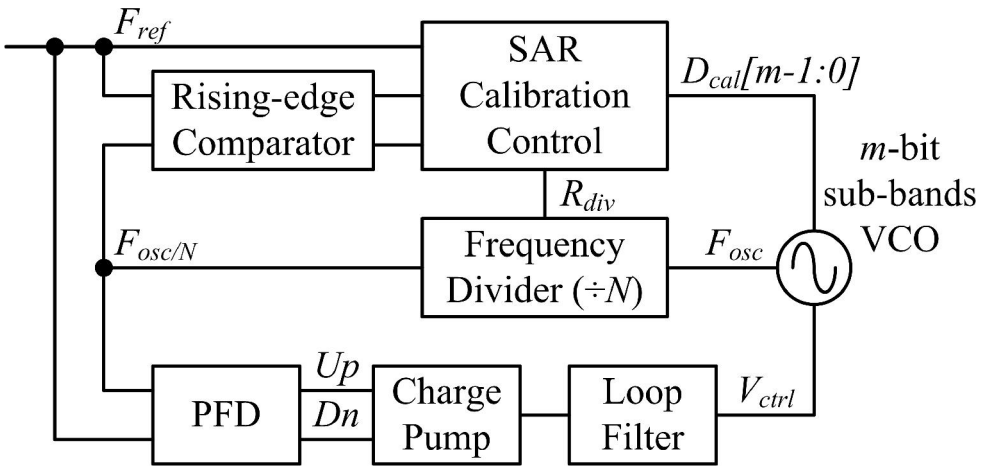

Figure 3.3. Block diagram of the frequency tuning loop for a wideband VCO with multiple sub-bands.

3.3 Frequency Calibration Circuit Design

Fast frequency calibration helps decrease the transmitter start-up time. For the start-up energy consumption to be minimal, the frequency calibration circuit must consume as little power as possible. This section presents a low-power implementation of this frequency calibration technique. Figure 3.4(a) displays the

block diagram of the circuit implementation, which contains two more blocks: a divide-by-2 block and an additional frequency divider.

The divide-by-2 block serves as a buffer for the oscillator and also converts a sinusoidal wave at the oscillation frequency (F_{osc}) into a square wave at half the oscillation frequency ($F_{osc/2}$). This eases the speed requirement of the frequency divider by a factor of two. However, the reference frequency must also be reduced by a factor of two to maintain the original frequency accuracy. As a consequence, the energy dissipation during the transmitter start-up period increases as the frequency calibration time is doubled.

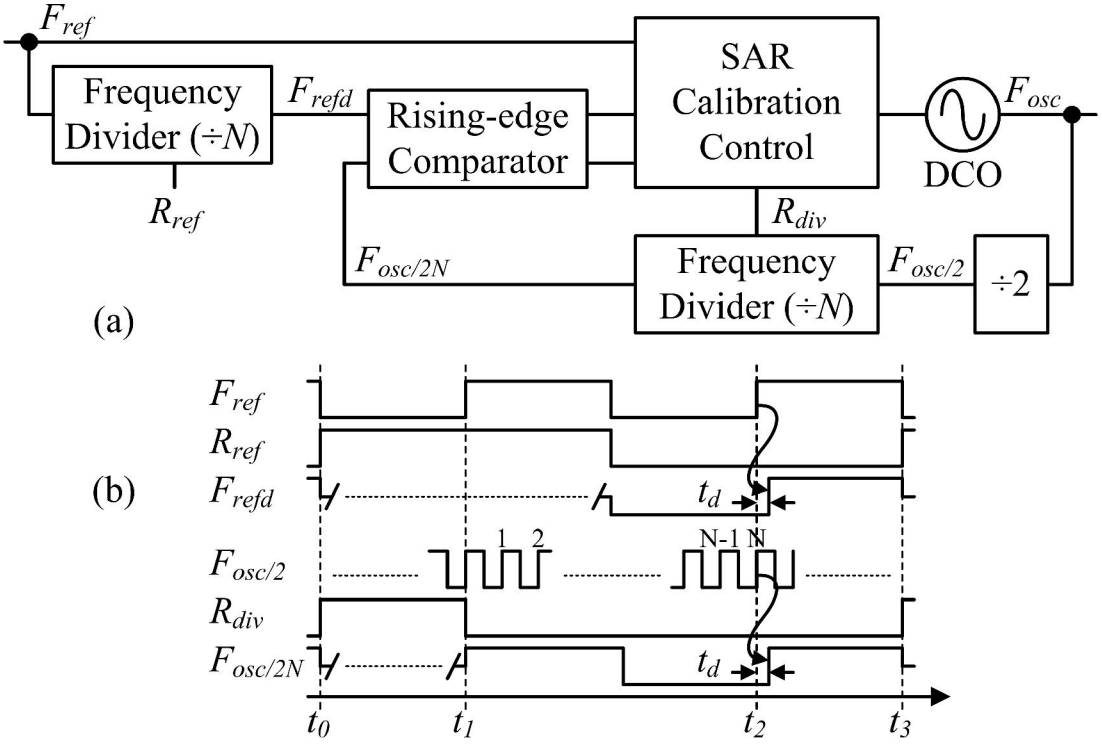

Figure 3.4. Circuit implementation of the fast frequency calibration loop. (a) Block, and (b) timing diagrams.

The additional frequency divider is inserted between the reference and the rising-edge comparator. The purpose of this block is not to divide the reference frequency but to add a delay time (t_d) to the rising edge of F_{ref}. This delay time equalizes the propagation delay of the main frequency divider when the N^{th} rising edge of $F_{osc/2}$ triggers the rising edge of $F_{osc/2N}$. The delay equalization is accomplished by adding the additional reference reset signal (R_{ref}) to the frequency divider. This R_{ref} forces the additional frequency divider to be under the same condition as the main frequency divider before triggering by the N^{th} rising edge of $F_{osc/2}$. The timing of these signals is depicted in Figure 3.4(b).

A. Divide-by-2 circuit

The low-power realization of the divide-by-2 circuit is shown in Figure 3.5. The differential sinusoidal input is squared up by two input inverters. The input frequency is then divided by three inverters connected as a ring oscillator with two transmission gates in between. Without these transmission gates, the ring oscillator output toggles at the period equal to twice the total delay of the ring oscillator loop. The two transmission gates with opposite input phases force the loop delay to equal the input period. Thus, the output of this circuit toggles at the period equal to twice the input period or at a frequency equal to half the input frequency.

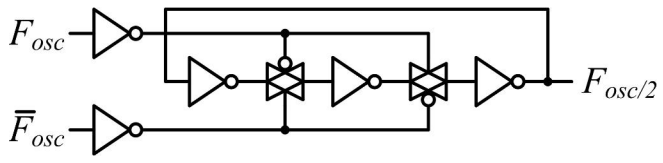

Figure 3.5. Schematic of the divide-by-2 circuit.

Of all the circuits in this frequency calibration technique, the divide-by-2 circuit operates at the highest frequency. To achieve high speed operation while consuming low amount of power, transistors are sized to have a high ratio of the transconductance to the parasitic capacitance. This allows the divide-by-2 circuit with an adequate supply voltage to operate at a high frequency. In this divider, no static power is consumed and the dynamic power due to switching is minimal because of a low parasitic capacitance design.

B. Frequency divider circuit with R_{div} and R_{ref}

The implementation of the frequency divider with R_{div} and R_{ref} is based on the truly modular programmable divider presented in [49]. This programmable divider is constructed by cascading p stages of divide-by-2/3 cells as shown in Figure 3.6. Its basic operation is similar to p-stage divide-by-2 cells in series where the output period (T_{out}) is 2^p times the input period (T_{in}). However, the modulus chain (M) in this programmable divider allows extra p periods to be added or not be added to $T_{out,}$ depending on the programmable control signal (P). Each of the extra periods is inserted when one of these cells is selected to be divide-by-3. The length of these p periods varies from $2^{p-1} \cdot T_{in}$ of the last cell down to $1 \cdot T_{in}$ of the first cell. Hence, T_{out} of this frequency divider can be written as:

$$T_{out} = \left(2^p + 2^{p-1} \cdot P_{p-1} + 2^{p-2} \cdot P_{p-2} + \ldots + 2 \cdot P_1 + P_0\right) \cdot T_{in} \tag{3.1}$$

Therefore, the frequency divider number (N), which is the ratio of T_{out} over $T_{in,}$ can be summarized as:

$$N = 2^p + P[p-1:0]. \tag{3.2}$$

The division range, which is defined by the minimum and the maximum N, is 2^p to 2^{p+1}-1 for $P = 0$ and $P = 2^p$-1, respectively. Because of the truly modular architecture of the frequency divider, the division range can be easily scaled by increasing or decreasing the number of cascaded stages. Moreover, the division range can be extended by a factor of two with only a few extra gates per stage as demonstrated in [50].

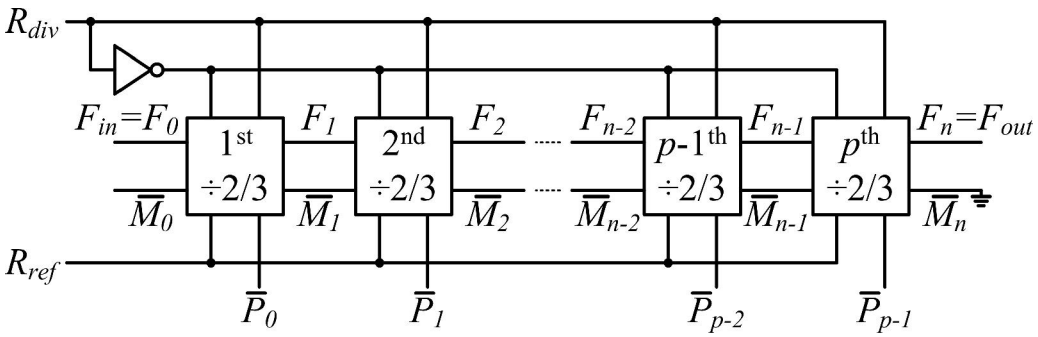

Figure 3.6. Architecture of the frequency divider circuit with R_{div} and R_{ref}.

Figure 3.7 represents the schematic of the divide-by-2/3 cell using logic gates. It consists of 4 D-latches and 5 gates. The upper two D-latches connected in a feedback loop function as a divide-by-2 circuit. The lower two D-latches control the insertion of the extra divide-by-3 period depending on M and P. These D-latches and gates are combined together as illustrated with dashed boxes and then realized by using the true single-phase-clocking (TSPC) technique [51] to minimize the number of transistors. Fewer transistors result in a smaller parasitic capacitance. As a result, the frequency divider presented in Figure 3.6 will operate at high speed and consume

low amounts of power. The transistor-level schematic of the divide-by-2/3 cell is depicted in Figure 3.8 with corresponding dashed boxes from Figure 3.7.

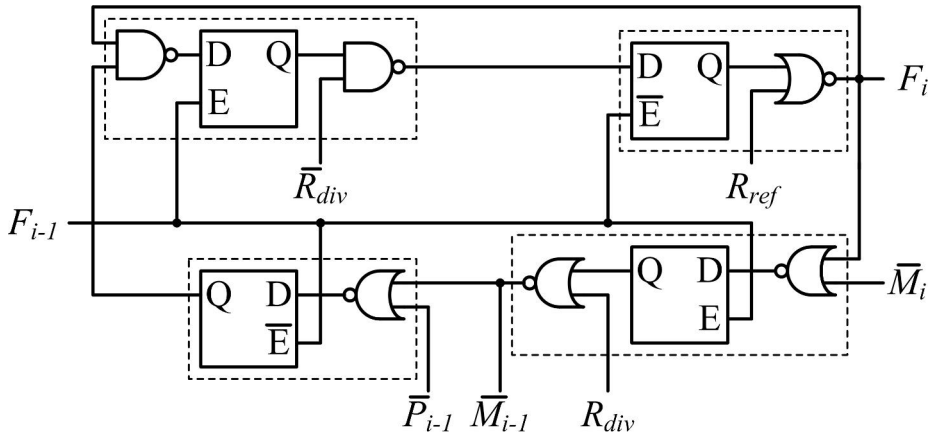

Figure 3.7. Logic-gate-level schematic of the divide-by-2/3 cell.

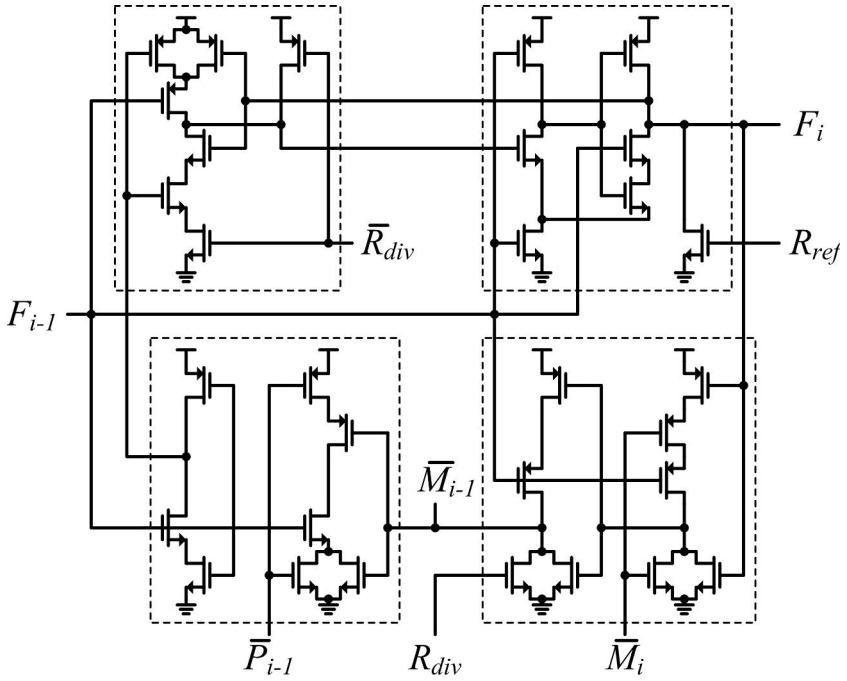

Figure 3.8. Transistor-level schematic of the divide-by-2/3 cell.

C. Rising-edge comparator circuit

The rising-edge comparator simply consists of two inverters with an additional NMOS cross-coupled pair inserted on top of the inverter NMOS, as shown in Figure 3.9. The input that rises first will toggle its output and disable the other output to be toggled when the other input rises. In this frequency calibration, one output indicates that the oscillation frequency is lower than $2 \cdot N$ times the reference frequency and the other output indicates the opposite.

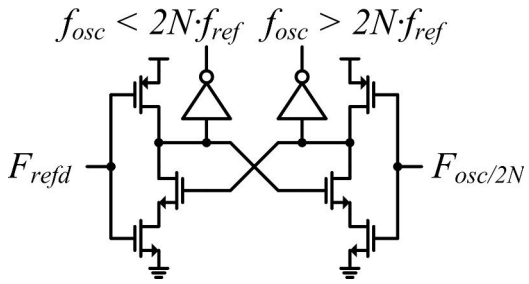

Figure 3.9. Schematic of the rising-edge comparator.

D. SAR calibration control

The SAR algorithm is utilized for frequency calibration of the DCO as shown in Figure 3.10. The algorithm starts by resetting the digital calibration value (D_{cal}) for the minimum oscillation frequency. After that, the MSB of D_{cal} is set for a higher frequency. Then the frequency comparison is made by generating R_{div} and R_{ref} as illustrated in Figure 3.4(b). If the oscillation frequency is higher than the desired frequency, the MSB is reset. This frequency comparison repeats from the MSB to the LSB of D_{cal}, and the oscillation frequency converges closest to the desired frequency on the final D_{cal}. The calibration control circuit is simply synthesized using logic-

gate standard cells. The power consumption of the calibration control circuit is negligible since it operates at a relatively low speed.

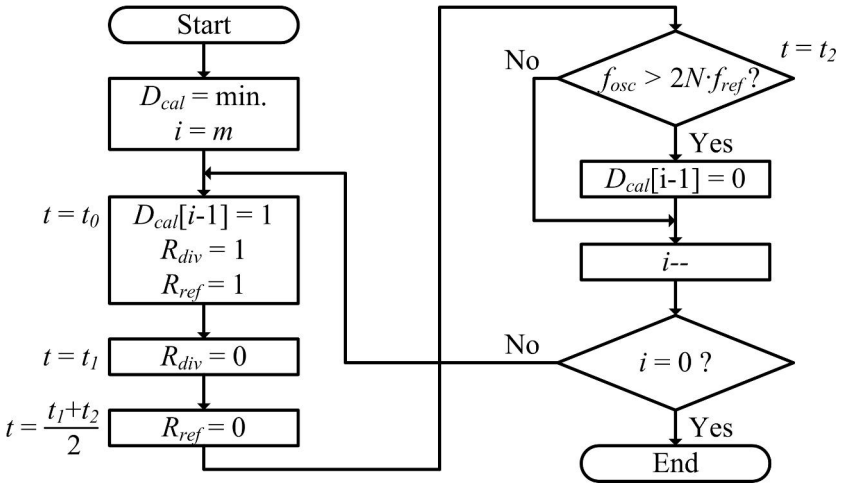

Figure 3.10. Flow chart of the SAR calibration control.

3.4 Transmitter Circuit Design

The prototype WSN transmitter with fast frequency calibration is designed to pair with the super-regenerative receiver in [44]. The transmitter employs the direct modulation architecture for low energy consumption as described in Section 2.4. The transmitter block diagram is depicted in Figure 3.11. In addition to the frequency calibration circuit, the transmitter contains an oscillator, a power amplifier with an impedance transformer, and digital control. The oscillator generates an RF frequency for the 915-MHz ISM band as a carrier signal. It alternates between two RF frequencies to represent the BFSK modulation data. The power amplifier is used to drive the antenna for an efficient delivery of the radiated power around -3 dBm. The digital control manages two frequency calibrations for BFSK modulation and

provides the data serial interface as well. The following subsections describe each of these blocks in detail.

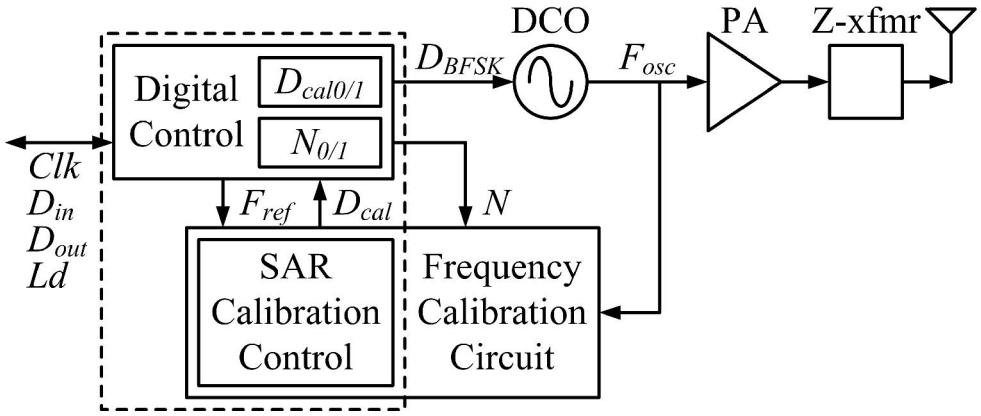

Figure 3.11. Block diagram of the 915-MHz WSN transmitter.

A. Oscillator

The schematic of the digitally controlled oscillator is displayed in Figure 3.12. The oscillator is made of PMOS and NMOS cross-coupled pairs and an LC resonator. The oscillator output is centered at the middle of the supply voltage. Therefore, it can directly connect to the divide-by-2 circuit of the frequency calibration block without the need for any biasing circuit. The oscillation frequency (f_{osc}) is expressed as:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}. \tag{3.3}$$

The inductance is implemented by a single 10.4-nH off-chip inductor. Using the off-chip inductor is much cheaper than fabricating a large on-chip inductor at 915 MHz. More importantly, it minimizes the oscillator power consumption due to its higher

quality factor (Q). The capacitance consists of 8-bit binary-weighted varactors plus another MSB varactor. The combination of these varactors creates 384 different capacitance values and hence 384 oscillation frequencies. The oscillator is designed to oscillate from 820 to 1010 MHz with a frequency step of approximately 0.5 MHz. This oscillation range covers the 915-MHz ISM band (902-928 MHz) with ± 9 % margin in order to tolerate inductor and varactor variations. The oscillator has a frequency step of approximately 0.5 MHz. This is two times smaller than the frequency calibration accuracy of 1 MHz. Thus, the frequency accuracy of the transmitter is dominated by the frequency accuracy of the frequency calibration.

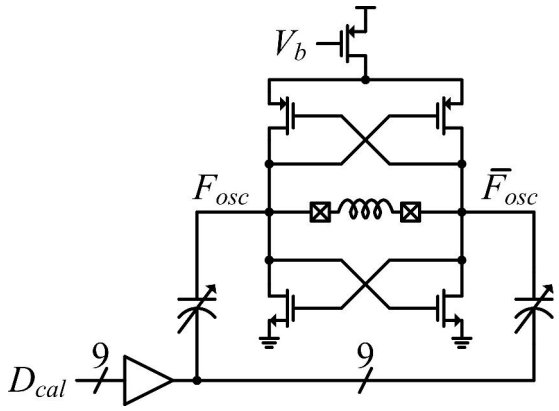

Figure 3.12. Schematic of the digitally controlled oscillator.

B. Power amplifier with an impedance transformer

Figure 3.13 shows the schematic of the power amplifier with an impedance transformer. The pseudo differential driver is comprised of both PMOS and NMOS transistors. Each transistor is biased so that it conducts current for only half of the oscillation period. This is the same as a push-pull amplifier, which has a theoretical

peak efficiency of 78 % at the maximum output swing. The impedance transformer is formed by an LC matching network and a balun. It increases the antenna resistance (R_{ant}) seen by the driver in order for the driver to deliver the desired -3 dBm radiated power with peak efficiency at the maximum output swing.

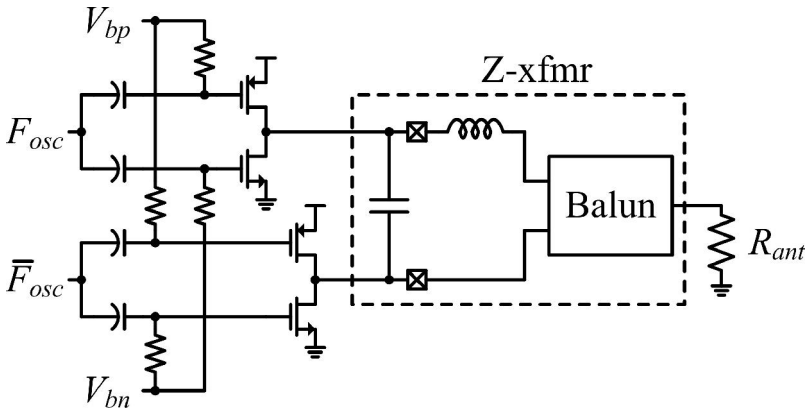

Figure 3.13. Schematic of the power amplifier with an impedance transformer.

C. Frequency calibration circuit and digital control

The frequency calibration circuit as described in Section 3.3 is implemented by cascading 9 divide-by-2/3 cells as the frequency divider. These 9 cells give the programmable control signal (P) a total of 9 bits and hence the divider number (N) from (3.2) of 512-1023. However, the top 3 bits are marked as a '110' constant since only the last 6 bits are sufficient to cover the 915-MHz ISM band with F_{ref} of 0.5 MHz. In this case, N is shrunk down to 896-959 and the calibrated frequency can be specified as 896-959 MHz with 1-MHz increments. The 0.5-MHz F_{ref} is chosen to limit the calibration frequency accuracy to 1 MHz. This accuracy is sufficient for the

transmitter since it is still lower than the input bandwidth of the intended receiver in [44].

The SAR calibration control and the digital control, labeled by the dashed box in Figure 3.11, are written in VHDL and synthesized using logic-gate standard cells. First, the digital control resets the transmitter and then initializes two *N*s that correspond to the two BFSK frequencies. After that, the digital control calibrates the oscillator twice and keeps two digital control codes (D_{cal}) as the result. Finally, the digital control transmits the BFSK data by multiplexing the oscillation frequency through these two D_{cal} codes.

3.5 Measurement Results

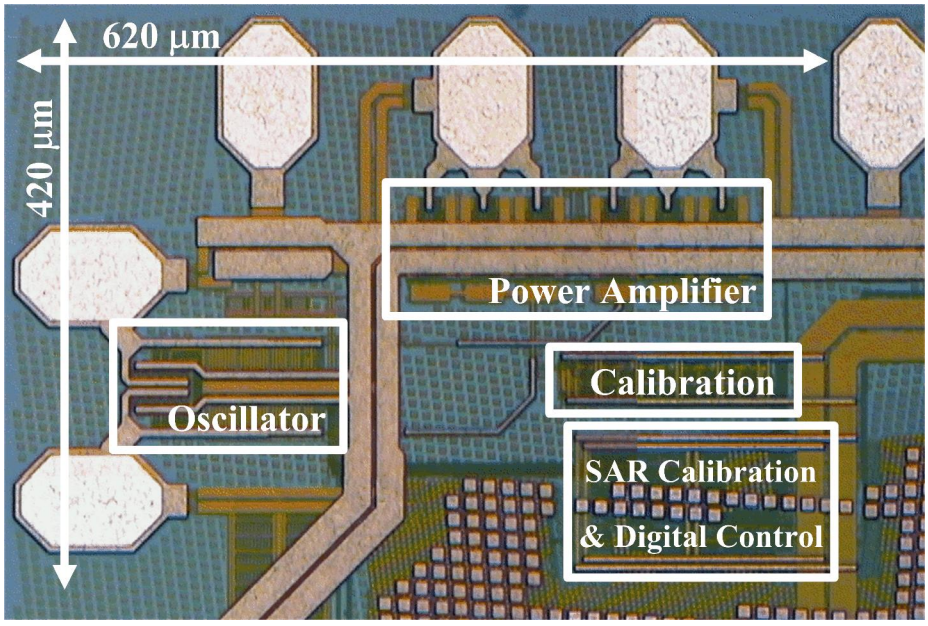

Figure 3.14. Die photograph of the transmitter.

The prototype transmitter was fabricated in a 0.18-µm CMOS process and occupies an active area of only 0.25 mm^2, excluding the power supply and digital control pads. Figure 3.14 shows the die photograph of the transmitter. The oscillator pads and the power amplifier pads are positioned to be bonded perpendicularly in order to minimize RF coupling.

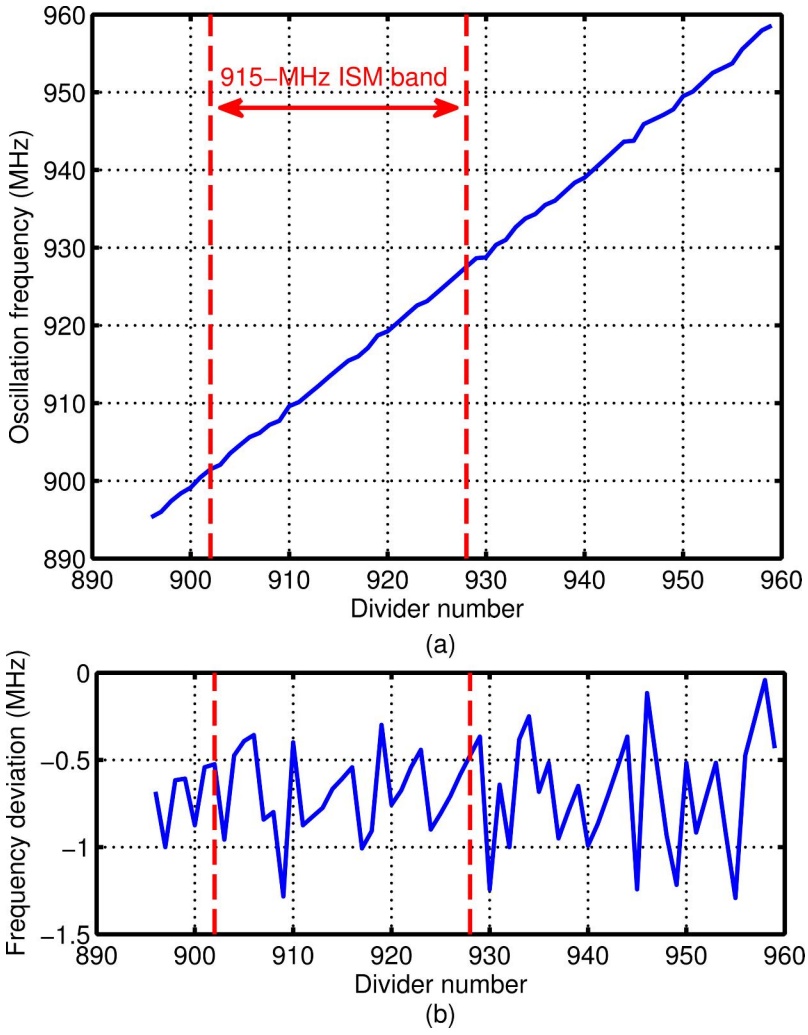

Figure 3.15. Measured calibrated frequency with divider number sweep. (a) Oscillation frequency. (b) Frequency deviation.

One frequency calibration of the 9-bit DCO takes 18 clock cycles. Thus, to complete two frequency calibrations for BFSK modulation, 36 clock cycles are required. This translates to a fast calibration time of 72 μs with a 0.5-MHz F_{ref}. The calibrated frequency is plotted in Figure 3.15(a). It linearly increases as the divider number increases. Most calibrated frequencies are in the range $2\cdot(N\text{-}1)\cdot F_{ref}$ and $2\cdot N\cdot F_{ref}$. In other words, they deviate within the range of the 1-MHz frequency accuracy as shown in Figure 3.15(b). However, some calibrated frequencies of this transmitter exceed the lower bound. This additional frequency deviation is caused by the frequency step limitation of the DCO. The frequency deviation will be closer to the systematic frequency accuracy as the DCO frequency step becomes smaller.

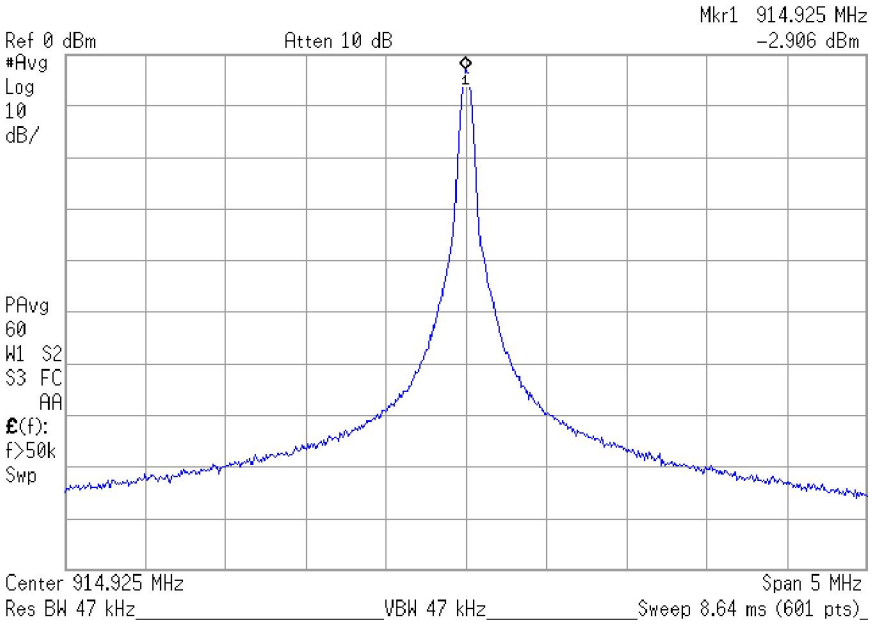

Figure 3.16. Measured output spectrum at 915 MHz.

The transmitter operates with a 0.9-V supply. The frequency calibration circuit draws power that is less than 100 μW and can be disabled during a data transmission period. The oscillator consumes about 410 μW. It oscillates from 864 MHz to 1.06 GHz, slightly higher than the design but still within the tolerance margin. The power amplifier outputs -2.9 dBm of radiated power while dissipating 1.50 mW. This corresponds to a power amplifier efficiency and transmitter efficiency of 34 % and 27 %, respectively. Figure 3.16 displays the output spectrum at 915 MHz. The transmitter oscillator exhibits good phase noise as low as -122 dBc/Hz at a 1-MHz offset frequency.

In addition, the prototype transmitter is capable of communicating with an OOK receiver by turning on and off the transmitter output. The output is turned on and off by enabling and disabling the bias voltage control of the oscillator and power amplifier. The on and off times as depicted in Figure 3.17 are 120 and 70 ns, respectively. If these transition times are assumed to be equal to 10 % of a bit period, the transmitter can transmit OOK modulation data up to 1 Mbps. Moreover, the calibration time is reduced by a factor of two as only one frequency calibration is required.

Table 3.1 summarizes the key performance parameters of this prototype transmitter and provides a comparison with other low-power WSN transmitters. This transmitter has high efficiency and a short frequency tuning time. This reduces the energy dissipation during start-up of the transmitter.

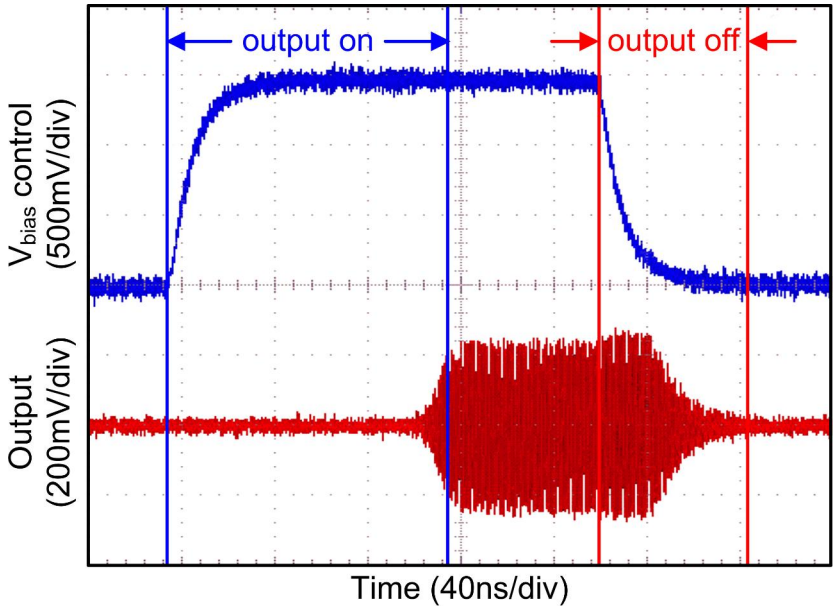

Figure 3.17. Measured output transient with bias voltage control.

Table 3.1. Performance summary of the prototype transmitter and comparison to other low-power WSN transmitters.

	[7]	[8]	[38]	[40]	This work
Technology (μm)	0.25	0.13	0.13	0.25	0.18
Frequency (MHz)	915	2450	1900	434	915
Supply voltage (V)	1.2	0.4	1.0	1.3	0.9
Radiated power (dBm)	-6.0	-5.2	0	0	-2.9
Power consumption (mW)	1.3	1.0	3.6	5.0	1.91
Transmitter efficiency (%)	19	30	28	20	27
Frequency tuning time and reference frequency	-	-	-	200 μs 8 MHz	72 μs 0.5 MHz

3.6 Summary

The design of an ultra-low-energy transmitter for wireless sensor networks is presented. The transmitter design incorporates a fast frequency calibration to reduce the frequency tuning time. This minimizes the energy consumption during the transmitter start-up period.

The prototype transmitter was fabricated in a 0.18-μm CMOS technology. It is capable of modulating both OOK and BFSK data on to the 915-MHz ISM band. By using a direct modulation architecture, the transmitter consumes power as low as 1.91 mW while efficiently radiating a power of -2.9 dBm.

4. A 2.4-GHZ HIGH-EFFICIENCY WSN TRANSMITTER USING A POWER OSCILLATOR

4.1 Introduction

Wireless sensor networks (WSNs) are becoming more widely used to monitor systems. In order to be suitable for a variety of applications, miniature sensor nodes must be developed. For ultra-low-energy sensor nodes, energy harvesting can be used as an energy source instead of a battery. This creates a battery-free WSN which has virtually limitless lifetime. To achieve the low level of energy consumption, WSN transmitters, the most dominant source of energy consumption in sensor nodes, should be designed to consume the lowest possible energy.

The energy consumption of WSN transmitters can be significantly reduced by utilizing a high efficiency transmitter. However, designing a high efficiency transmitter for WSNs is difficult because of the relatively low radiated power levels. The radiated power of WSN transmitters is low as the communication distance between sensor nodes is fairly short. As a result, a small amount of power loss in the transmitter can decrease the transmitter efficiency significantly. The transmitter power loss must be minimized in order to achieve a high transmitter efficiency.

This chapter demonstrates the design of a 2.45-GHz WSN transmitter operating with a single supply of 0.65 V. The presented transmitter employs a power oscillator architecture [38] to decrease the transmitter power loss. The efficiency of the power oscillator circuit is analyzed and a detailed design procedure is developed. This

procedure provides guidelines for maximum efficiency and an optimal supply voltage.

4.2 Power Oscillator Architecture

In a conventional direct modulation architecture reviewed in Section 2.4, an oscillator and a power amplifier are designed separately to serve as a frequency generator and an antenna driver, respectively. A power oscillator architecture combines these two circuits. Thereby the power loss is lowered since the same power is consumed for both the oscillating and antenna driving functions. This power loss reduction helps improve the transmitter efficiency, particularly for WSN transmitters where the power consumption is typically low.

Figure 4.1 displays the schematic of the power oscillator circuit. It consists of an LC oscillator with an impedance transformer and an antenna as a part of its resonant load. In this circuit, an NMOSFET cross-coupled pair produces the oscillation. The oscillation frequency is determined by the inductance, the varactor capacitance, and the impedance transformer capacitance. The varactor DC voltage (V_{var}) is used to control the frequency of oscillation. The impedance transformer which consists of two capacitors is used to boost the resistance of the 50-Ω antenna seen by the oscillator. This effective resistance allows the oscillator to operate at the maximum achievable efficiency while delivering a desired radiated power to the antenna.

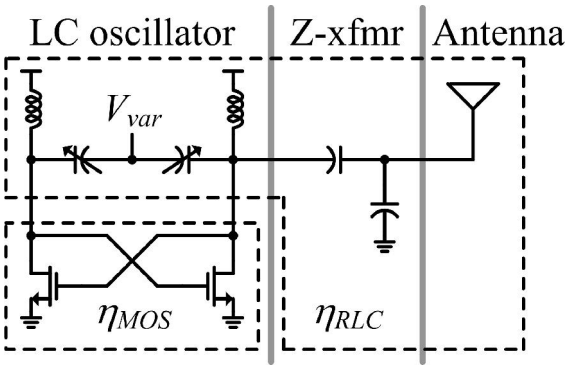

Figure 4.1. Schematic of the power oscillator circuit.

The shortcoming of the power oscillator architecture is a variation in the oscillation frequency. The antenna impedance in reality is not a constant and it varies depending on its surrounding environment. As a result, the oscillation frequency may drift over a period of time since the antenna is part of the oscillator load. For this reason, the power oscillator architecture is particularly suitable for a short-duration communication such as WSNs where the antenna impedance is considerably constant over a single communication period.

4.3 Power Oscillator Efficiency Analysis

High efficiency is the primary focus of the power oscillator design. This section provides an analysis for the efficiency of the power oscillator. The analysis begins with partitioning the power oscillator circuit into two blocks illustrated by the two dashed boxes in Figure 4.1. The first block contains only the MOSFET cross-coupled pair while the other block contains the rest of the circuit which includes only RLC components. The efficiency of both blocks (MOSFET and RLC components) and the whole power oscillator are described as follows.

A. MOS transistor efficiency (η_{MOS})

The efficiency of the MOSFET cross-coupled pair driving the oscillator output can be evaluated through a single MOS transistor modeled in Figure 4.2(a). Because of the oscillation, the voltages across the gate-source (V_{gs}) and drain-source (V_{ds}) terminals can be considered as an ideal sinusoid with opposite phases and are expressed by:

$$\begin{aligned} V_{gs} &= V_{dd} + V_i \cos \omega t \\ V_{ds} &= V_{dd} - V_o \cos \omega t \end{aligned} \tag{4.1}$$

where V_{dd} is the DC bias voltage which in Figure 4.1 equals the supply voltage, V_i and V_o are the amplitudes of the sinusoidal V_{gs} and V_{ds}, respectively, and ω is the oscillation frequency. The current flowing into the drain terminal (I_d) based on the first-order model of MOSFET current-voltage characteristics can be written as:

$$\begin{aligned} I_{d,tri} &= k \frac{W}{L}\left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds} && |\theta| \le \alpha \\ I_{d,sat} &= \frac{k}{2}\frac{W}{L}\left(V_{gs} - V_{th} \right)^2 && \alpha < |\theta| \le \beta \\ I_{d,cut} &= 0 && \beta < |\theta| \end{aligned} \tag{4.2}$$

where $\theta = \omega t$ is the angular phase, k is a process parameter, V_{th} is the MOSFET threshold voltage, W and L are width and length of the MOS transistor, α and β are the angular phase boundaries between linear/saturation and saturation/cut-off regions of the MOS transistor, respectively. α and β are defined by:

$$\alpha = \cos^{-1}\left(\frac{V_{th}}{V_i + V_o}\right)$$
$$\beta = \cos^{-1}\left(\frac{V_{th} - V_{dd}}{V_i}\right). \tag{4.3}$$

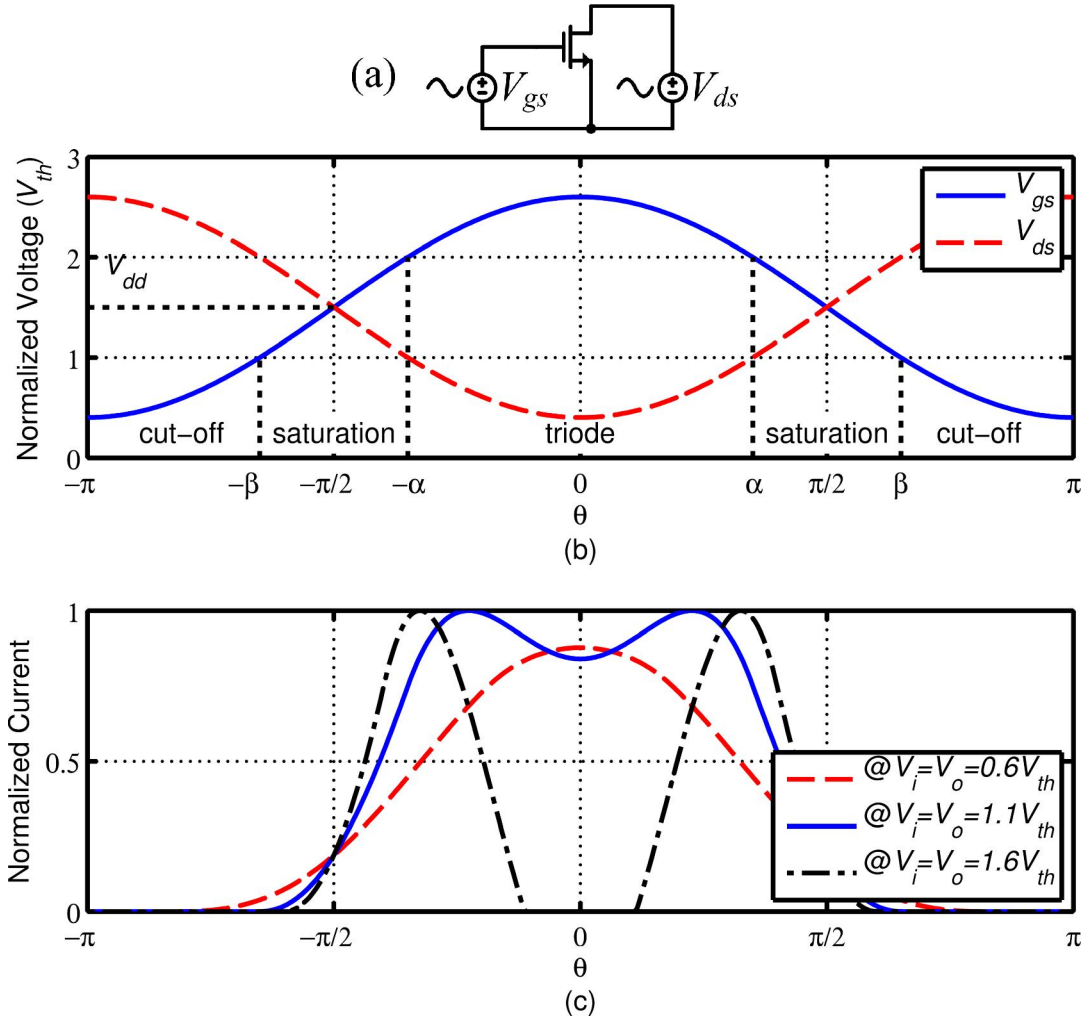

Figure 4.2. (a) MOS transistor of the power oscillator. (b) Associated voltage, and (c) current waveforms (V_{dd} = 1.5·V_{th}, V_i = V_o = 1.1·V_{th} for voltage, and V_i = V_o = 0.6/1.1/1.6·V_{th} for current).

Figure 4.2(b) shows an example of V_{gs} and V_{ds} when V_{dd} = 1.5·V_{th} and V_i = V_o = 1.1·V_{th}. The corresponding I_d, normalized to its maximum value, is plotted in Figure

4.2(c). Two additional drain currents when $V_i = V_o = 0.6 \cdot V_{th}$ and $V_i = V_o = 1.6 \cdot V_{th}$ are provided for comparison. These three drain currents represent three different aspects of the MOS transistor efficiency. At small sinusoidal amplitudes ($0.6 \cdot V_{th}$), the amplitude of the drain current and hence the efficiency are low. The efficiency increases as these voltages and thus the drain current amplitudes increase ($1.1 \cdot V_{th}$). However, too large of an amplitude ($1.6 \cdot V_{th}$) causes a distortion in the drain current waveform and therefore decreases the efficiency.

The average drain current (I_{dc}) and the power consumption (P_{dc}) of this MOS transistor can be expressed by:

$$\begin{aligned} I_{dc} &= \frac{1}{2\pi}\left[\int_{-\pi}^{\pi} I_d d\theta\right] \\ &= \frac{1}{\pi}\left[\int_{0}^{\alpha} I_{d,tri} d\theta + \int_{\alpha}^{\beta} I_{d,sat} d\theta\right] \\ P_{dc} &= I_{dc} \cdot V_{dc}. \end{aligned} \tag{4.4}$$

The drain current fundamental amplitude (I_o) at the oscillation frequency and the output power (P_o) of this MOS transistor are similarly derived by:

$$\begin{aligned} I_o &= \frac{1}{\pi}\left[\int_{-\pi}^{\pi} I_d \cos\theta d\theta\right] \\ &= \frac{2}{\pi}\left[\int_{0}^{\alpha} I_{d,tri} \cos\theta d\theta + \int_{\alpha}^{\beta} I_{d,sat} \cos\theta d\theta\right] \\ P_o &= \frac{I_o \cdot V_o}{2}. \end{aligned} \tag{4.5}$$

The MOS transistor efficiency (η_{MOS}) is then determined as:

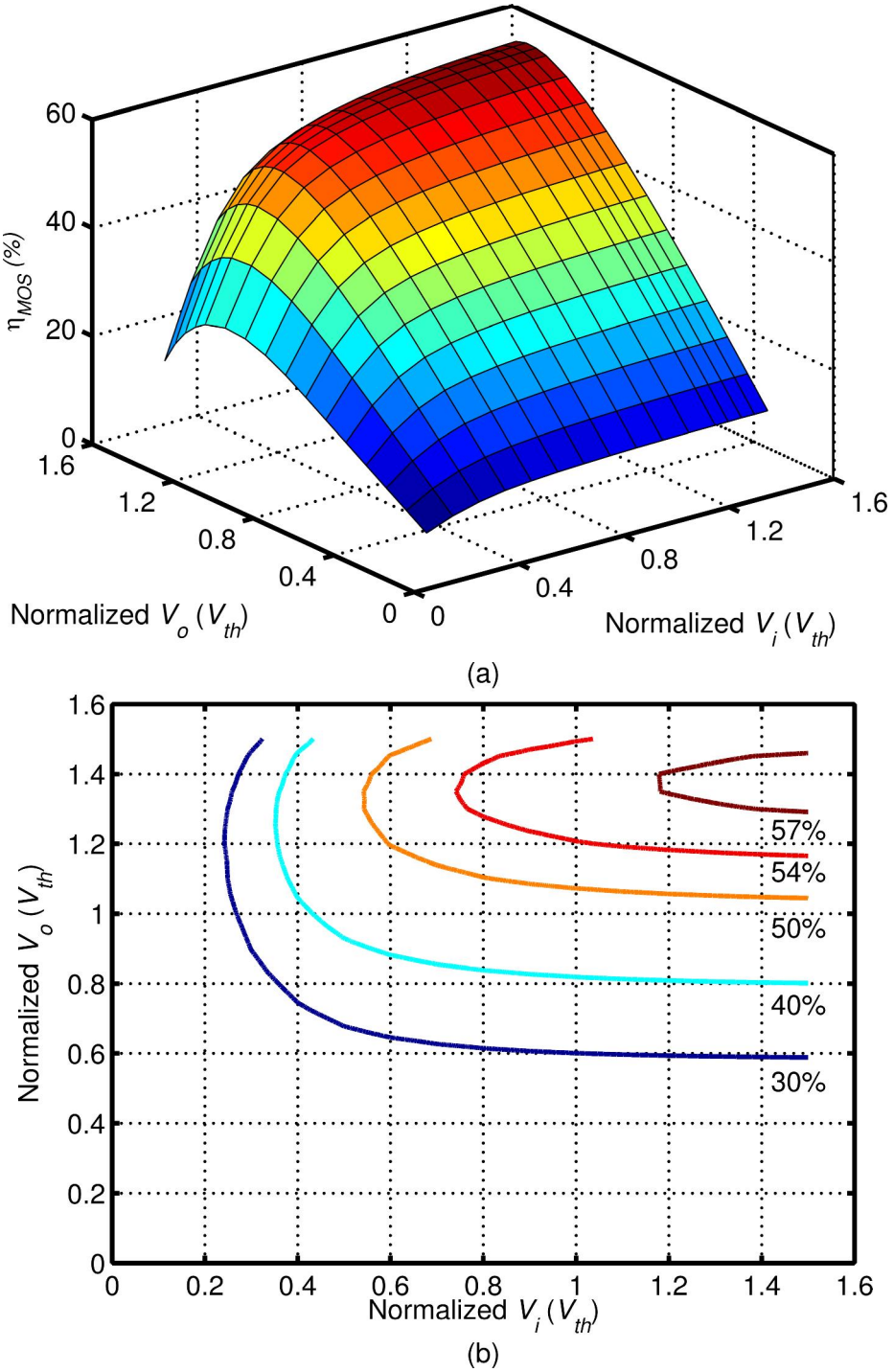

Figure 4.3. MOS transistor efficiency (a) surface, and (b) contour vs. input and output sinusoidal amplitudes ($V_{dd} = 1.5 \cdot V_{th}$).

$$\eta_{MOS} = \frac{P_o}{P_{dc}}. \tag{4.6}$$

Figure 4.3(a) illustrates the η_{MOS} surface with $V_{dd} = 1.5 \cdot V_{th}$ for a wide range of V_i and V_o normalized to V_{th}. The corresponding contour plots are shown in Figure 4.3(b). For the MOSFET cross-coupled oscillator, both V_i and V_o sinusoidal amplitudes are equal ($V_i = V_o$). As a result, the plot of η_{MOS} can be simplified as depicted in Figure 4.4. The efficiency of the MOSFET part of the oscillator increases as the oscillation amplitude (V_{osc}) increases. However, it reaches a maximum at 57.6 % and then decreases because of the drain current waveform distortion as previously shown in Figure 4.2(c). The drain current fundamental amplitude decreases and hence lowers the oscillation output power and η_{MOS}.

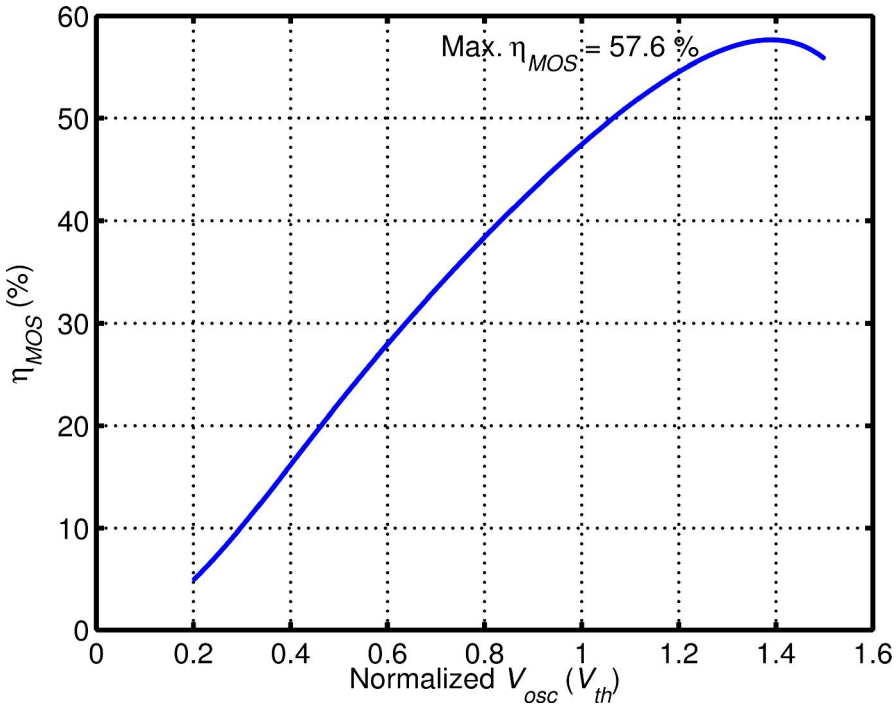

Figure 4.4. MOS transistor efficiency vs. oscillation amplitude ($V_{dd} = 1.5 \cdot V_{th}$).

The maximum value of η_{MOS} depends on the supply voltage. Figure 4.5 plots the maximum η_{MOS} for various supply voltages. A lower supply voltage yields a higher maximum efficiency. However, the output power capability for a given transistor width is also reduced as the supply voltage is lowered. Thus, for a given output power, a lower supply oscillator requires a wider transistor, which in turn increases the parasitic capacitance. In addition, the transistor's transconductance is also decreased. The increased capacitance and decreased transconductance affect the oscillation frequency and the oscillator start-up condition. Both of these characteristics must be taken into account when designing the power oscillator. The oscillation amplitude where η_{MOS} peaks also changes with the supply voltage. However, the change is approximately linear with the supply voltage. The oscillation amplitude at the maximum η_{MOS} varies in a narrow range of 92-96 % with supply voltage as shown in Figure 4.5.

The channel-length modulation of the MOS transistor can be incorporated into the efficiency analysis by multiplying I_d in (4.2) with the $(1+\lambda V_{ds})$ factor where λ is the channel-length modulation parameter. However, the effect of λ is small since the largest V_{ds} occurs when I_d is minimal. For $\lambda = 0.1$, the maximum η_{MOS} drops by less than 1 %.

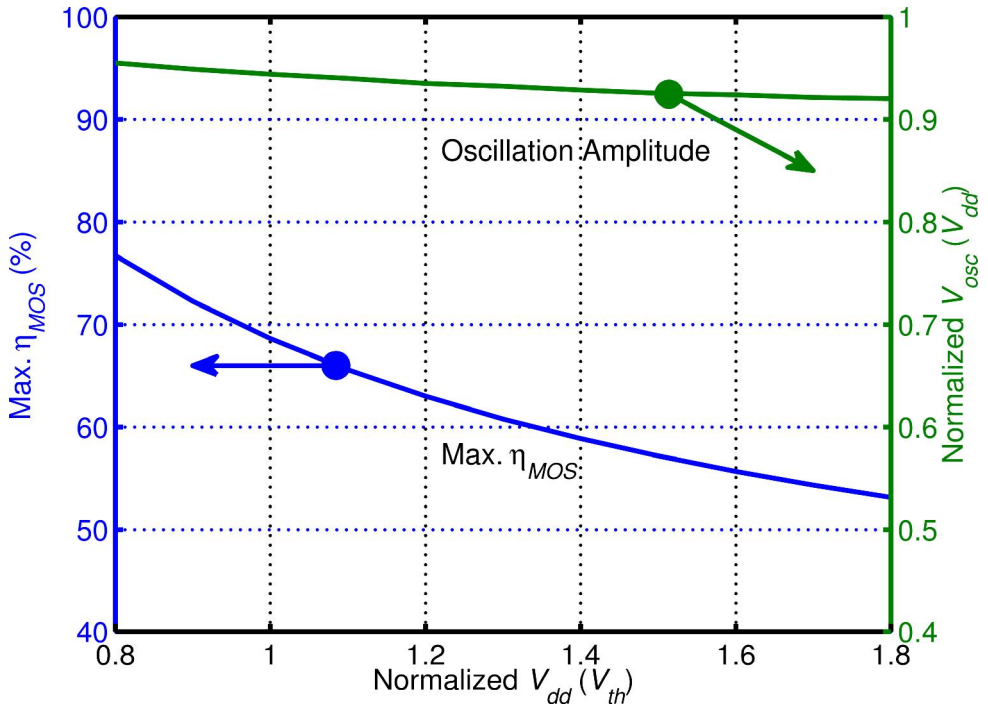

Figure 4.5. Maximum η_{MOS} and the oscillation amplitude vs. supply voltage.

B. RLC efficiency (η_{RLC})

The RLC block contains all the passive components of the power oscillator circuit including the inductor and the varactor of the oscillator, the impedance transformer, and the antenna. The simplified model of these components is shown in Figure 4.6. Losses in the inductor, varactor, and impedance transformer are represented by their respective conductances (G_{ind}, G_{var}, and $G_{z\text{-}xfmr}$). The power dissipated at the antenna or the radiated power (P_{rad}) which is delivered through the impedance transformer is represented by a conductance ($G_{ant\text{-}xfmr}$) as:

$$G_{ant-xfmr} = \frac{2P_{rad}}{V_{osc}^2}. \tag{4.7}$$

η_{RLC} is defined as the ratio of the radiated power to the total power dissipated. It can be written as:

$$\eta_{RLC} = \frac{G_{ant-xfmr}}{G_{ind} + G_{var} + G_{z-xfmr} + G_{ant-xfmr}}. \tag{4.8}$$

By substituting (4.7) in (4.8), it can be seen that η_{RLC} for a given radiated power exhibits a monotonic decrease as the oscillation amplitude increases.

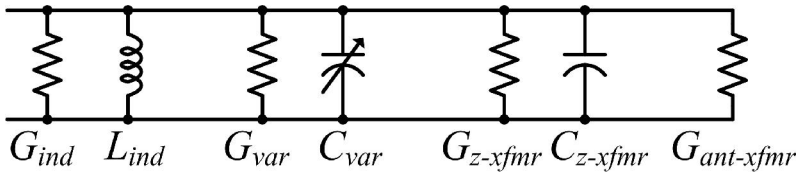

Figure 4.6. Simplified model of the passive components of the power oscillator.

C. Power oscillator efficiency (η_{POSC})

The efficiency of the power oscillator, which comprises the MOS transistor and RLC components, can be evaluated by multiplying together these two efficiencies as:

$$\eta_{POSC} = \eta_{MOS} \cdot \eta_{RLC}. \tag{4.9}$$

The power oscillator efficiency as a function of the oscillation amplitude will be similar to η_{MOS} shown in Figure 4.4 but with a lower value because of multiplication by η_{RLC}. The peak of the power oscillator efficiency also occurs at a lower oscillation amplitude than the peak of η_{MOS} due to the monotonic decrease of η_{RLC}.

Not every point on the power oscillator efficiency curve can be realized. In order for the oscillator to be realizable, the transistor's transconductance must be high enough to ensure oscillator start-up and the transistor's parasitic capacitance must be

low enough so that the maximum desired oscillation frequency can be achieved. These constraints will be applied while designing the power oscillator in the next section.

4.4 Power Oscillator Circuit Design

This section describes the design approach for a high efficiency, 2.45-GHz power oscillator circuit in a 0.18-μm CMOS process. First, the implementation and the design of the low-loss passive components are discussed. Then, the power oscillator circuit is designed based on the efficiency analysis of Section 4.3. The optimum supply voltage, which yields the highest achievable power oscillator efficiency, is then determined.

A. Passive components

Having low-loss passive components is important for a high efficiency design. At 2.45 GHz, the inductor is popularly realized by an on-chip inductor for high integration. However, the inductor for this power oscillator design is instead realized by a combination of bondwire and PCB trace inductances because of the need for a higher Q (lower loss). Unfortunately, the process variations of such an inductor are typically larger than an on-chip inductor. Therefore, the oscillator must be designed to have a wider tuning range to account for larger inductance variations.

8-bit binary-weighted varactors with an additional MSB varactor provide 384 capacitance values for the digital frequency tuning of the power oscillator. The oscillation frequency (f_{osc}) can be expressed as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{ind}\left(C_{MOS} + C_{z-xfmr} + C_{var1} + C_{var2} + \ldots + C_{var8} + C_{var9}\right)}} \tag{4.10}$$

where C_{MOS} is the MOSFET parasitic capacitance, L_{ind}, $C_{z\text{-}xfmr}$, and $C_{var1\text{-}9}$ are the oscillator inductance, the impedance transformer capacitance, and the varactor capacitances, respectively.

The tapped-capacitor impedance transformer, shown in Figure 4.7, is used to boost the antenna resistance loading for the oscillator for higher efficiency oscillation. When the C_2 impedance is comparable or smaller than the antenna resistance, the impedance transformation ratio (n^2) can be approximated as:

$$n^2 = \frac{R_{ant-xfmr}}{R_{ant}} \approx \left(\frac{C_1 + C_2}{C_1}\right)^2. \tag{4.11}$$

The tapped-capacitor structure is chosen as the impedance transformer for this power oscillator circuit because it provides an inherent DC blocking for the antenna. More importantly, the inductor can be omitted because of the inductance shared with the power oscillator. However, by sharing the inductance, the impedance transformer loads the power oscillator with a capacitance ($C_{z\text{-}xfmr}$) of

$$C_{z-xfmr} \approx \frac{C_1 C_2}{C_1 + C_2} = \frac{C_2}{n}. \tag{4.12}$$

For this transmitter, the C_2 capacitor is chosen as a fixed 1.3 pF to minimize the loading of the impedance transformer capacitance while still providing comparable impedance to the 50-Ω antenna. The C_1 capacitor and n are determined by the oscillation amplitude for maximum power oscillator efficiency.

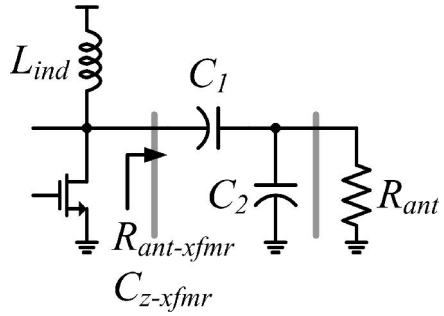

Figure 4.7. Schematic of the tapped-capacitor impedance transformer.

B. Power oscillator

In Section 4.3A, η_{MOS} is calculated based on the MOSFET current-voltage characteristics. The actual η_{MOS} for both NMOS and PMOS transistors of a specific 0.18-μm CMOS process can be verified by the circuit simulation setup shown in Figure 4.8. The efficiency is measured when the output resonant frequency is tuned to be exactly the same 2.45 GHz input frequency. This simulation setup also provides the transistor's transconductance and parasitic capacitance for a given transistor width. These two parameters are essential for verifying the oscillator start-up and the maximum oscillation frequency.

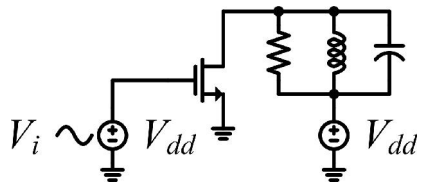

Figure 4.8. MOS transistor efficiency simulation circuit (NMOS).

Figure 4.9 presents η_{MOS} with a supply of 0.65 V. The peak efficiencies are 60.2 % and 54.8 % for NMOS and PMOS transistors, respectively. The NMOS

transistor has a higher peak efficiency than the PMOS transistor due to a higher threshold voltage in this process ($V_{th,NMOS}$ = 0.49 V and $V_{th,PMOS}$ = 0.43 V). These correspond to normalized V_{dd} of 1.33 and 1.51 which are very close to the efficiency analysis illustrated in Figure 4.5.

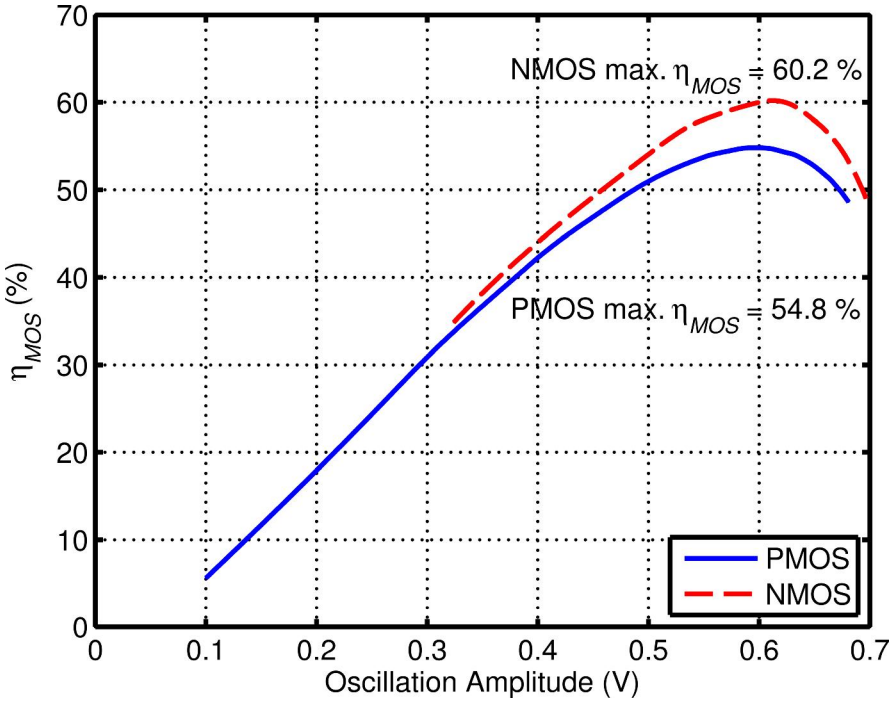

Figure 4.9. NMOS and PMOS transistor efficiencies vs. oscillation amplitude (V_{dd} = 0.65 V).

Although the use of PMOS transistors to implement the power oscillator tends to be inferior to the use of NMOS transistors considering η_{MOS}, a PMOSFET implementation is selected for this design because of the advantages offered in the varactor design. In the PMOS power oscillator, the varactor always operates with a negative DC voltage. Therefore, the varactor has a higher capacitance spread and higher Q than its NMOS counterpart as illustrated in Figure 4.10(b) [52]. The higher

capacitance spread implies that the varactor has a lower capacitance for the same difference between its maximum and minimum values. This allows the oscillator to operate at a higher frequency. The higher Q is directly related to lower loss.

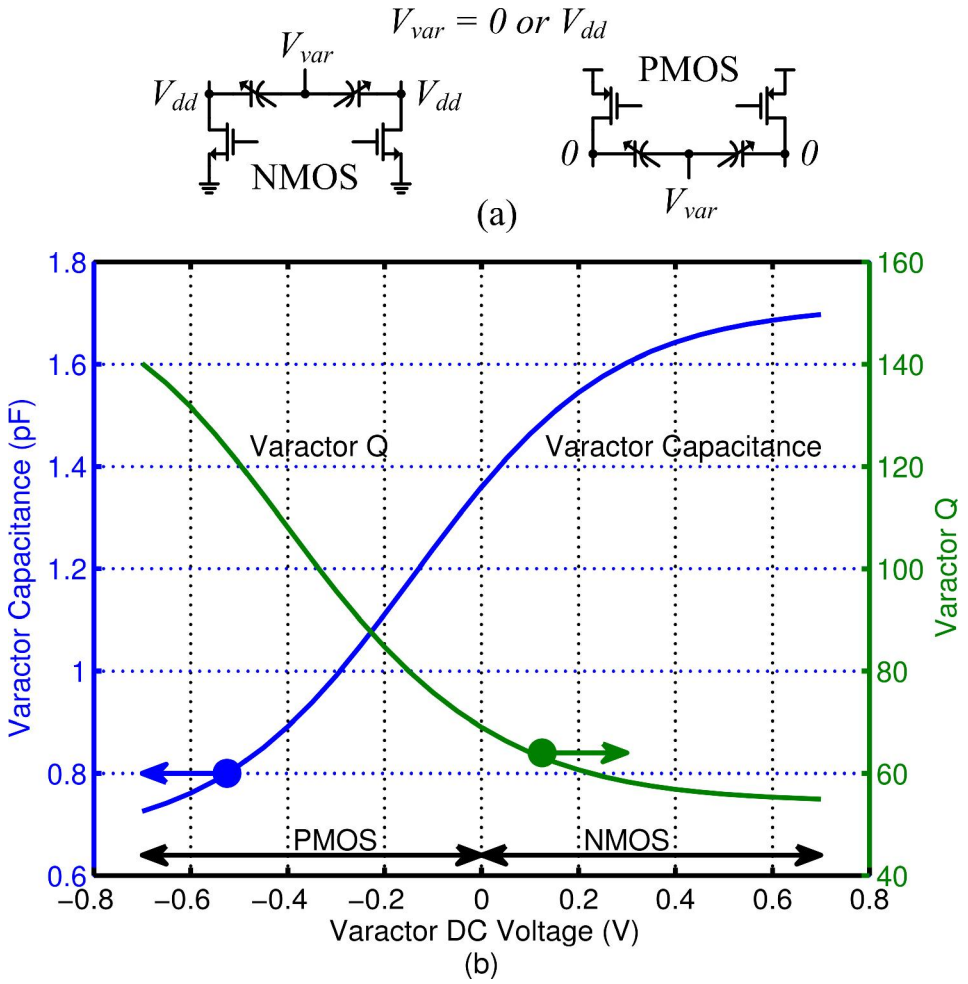

Figure 4.10. Comparison of varactor for NMOS and PMOS power oscillator. (a) DC voltages. (b) Capacitance and Q.

The loss of each passive component, represented by its conductance modeled in Figure 4.6, is plotted in Figure 4.11. Overall, the loss is dominated by the 2.17-nH inductor, followed by the varactor. There is virtually negligible loss from the

impedance transformer. Note that the varactor loss varies with the oscillation amplitude due to the varactor non-linearity. The varactor is normalized to have the same capacitance variation so that the range of the oscillation frequency with this inductor will be 2.31-2.59 GHz. This frequency range can tolerate inductor variations up to 8 %. Figure 4.11 also plots η_{RLC}. η_{RLC} is calculated based on a radiated power of 360 μW (-4.4 dBm) which would be sufficient for a communication distance of about 10-20 meters. As mentioned in Section 4.3, η_{RLC} monotonically decreases as the oscillation amplitude increases.

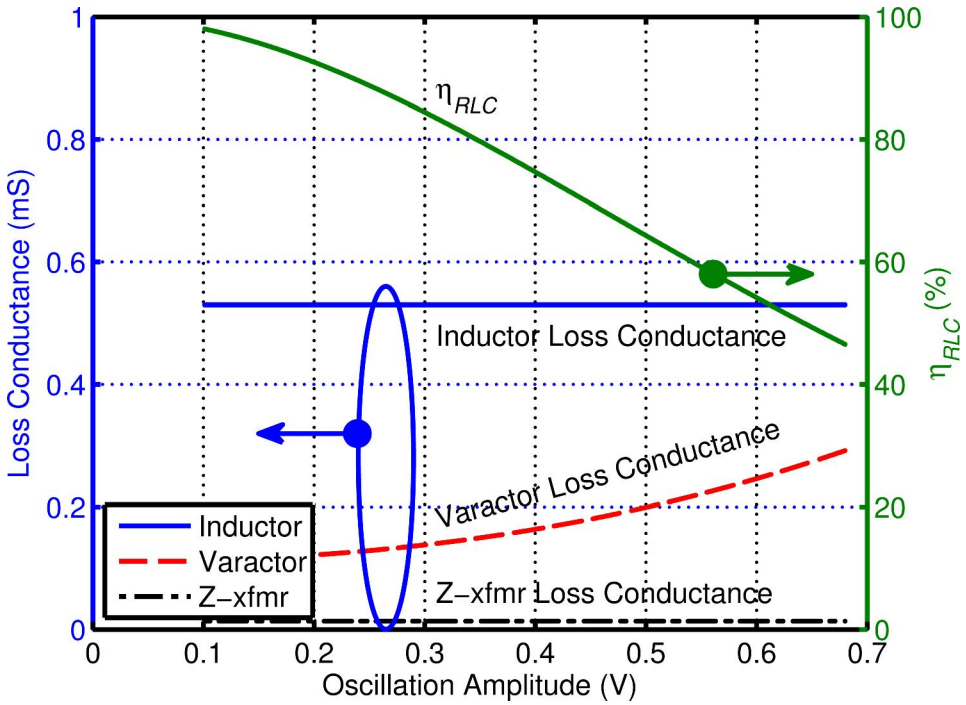

Figure 4.11. Loss conductance of the passive components and η_{RLC} vs. oscillation amplitude.

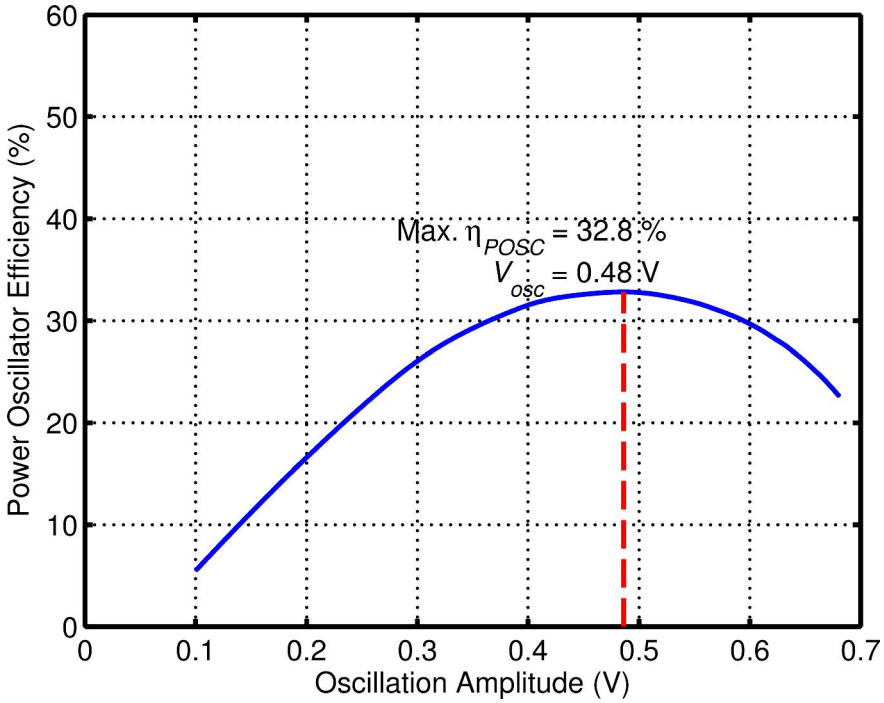

Figure 4.12. Power oscillator efficiency vs. oscillation amplitude.

The power oscillator efficiency is finally computed by multiplying η_{MOS} of the PMOS transistor from Figure 4.9 and η_{RLC} from Figure 4.11. The result is depicted in Figure 4.12. The efficiency of the power oscillator is maximized at 32.8 % when the oscillation amplitude is 0.48 V. The loop gain, a product of the transistor's conductance and its load, and the PMOS transistor width are plotted in Figure 4.13. At this particular amplitude, the loop gain is 1.8 and ensures that the power oscillator will build up oscillations. The transistor parasitic capacitance is calculated from the transistor width. It is combined with other capacitances in (4.10) to ensure that the desired maximum oscillation frequency of 2.59 GHz is still achievable. The

maximum efficiency power oscillator can be realized as these two conditions are met.

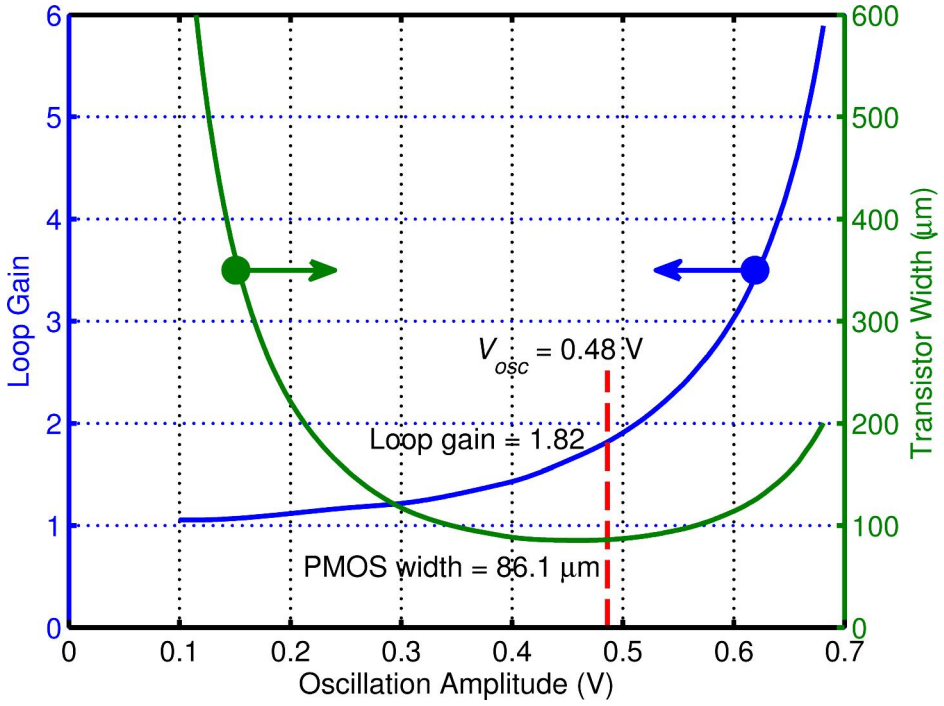

Figure 4.13. Loop gain and PMOS transistor width vs. oscillation amplitude.

C. Optimum supply voltage

Previously, the maximum power oscillator efficiency was evaluated based on a supply of 0.65 V. However, as pointed out by the mathematical efficiency analysis depicted in Figure 4.5, the maximum efficiency increases when the supply voltage decreases. The design procedure described previously is applied to other power oscillator designs with the same specifications but different supply voltages. Figure 4.14 shows the power oscillator efficiency as supply voltage is varied from 0.45 to 0.7 V with a 0.05 V increment. Two additional curves are shown in this figure. One

represents an oscillator loop gain of 1.7 and the other represents the maximum oscillation frequency of 2.59 GHz. The intersection of these two curves defines the shaded region in which the power oscillator can be designed to meet both the requirements. The top of this region, point A in Figure 4.14, indicates the maximum power oscillator efficiency that can be achieved for an optimum supply voltage. In this case, the maximum efficiency is increased to 38.5 % with an optimum supply voltage of approximately 0.55 V.

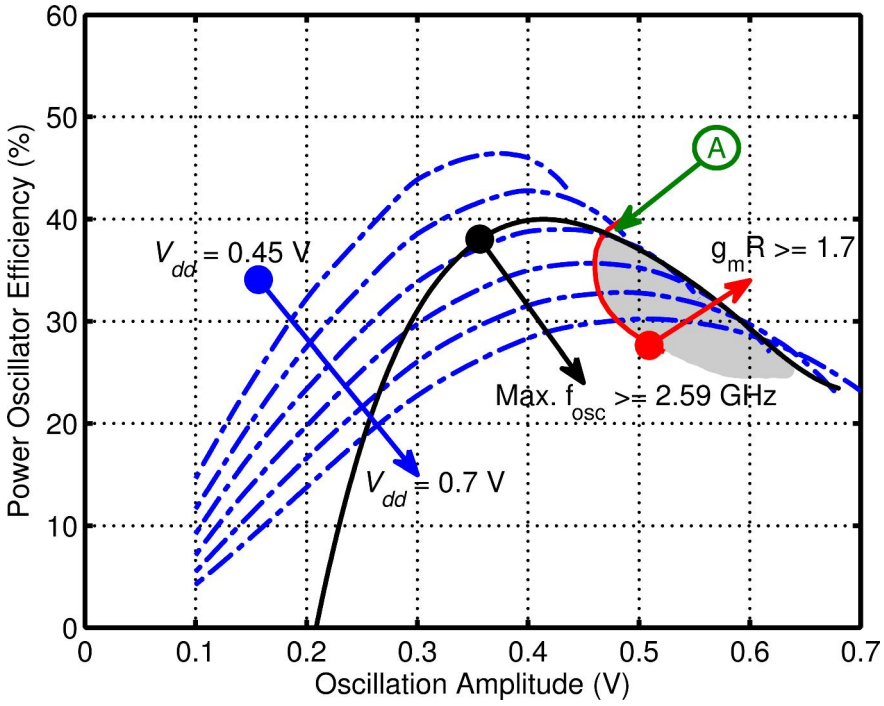

Figure 4.14. Optimum supply voltage for maximum power oscillator efficiency.

4.5 High-Efficiency Transmitter Circuit Design

This section describes the implementation of the power oscillator transmitter with a 0.65 V supply. The prototype transmitter employs the power oscillator design

with a sub-optimal supply voltage in order for the power oscillator supply voltage to be compatible with the rest of the transmitter circuitry. Since this supply voltage is the same as that of the intended receiver in [14], both can be integrated as a single-supply transceiver.

A. Power oscillator

Figure 4.15 shows the schematic of the prototype power oscillator transmitter. It is designed as a single-ended transmitter to directly drive a single-ended antenna. The PMOS transistor width in Figure 4.13 is calculated based on all loads of the power oscillator and thus is the total width of both M_1 and M_2 transistors. The width of each PMOS transistor depends on its load. Since the antenna is connected to only one side of the power oscillator, the two PMOS transistors see different loads. On the F_{osc-} side, the load is due to the losses in the inductor and varactor. On the F_{osc+} side, the load is due to the same losses plus losses in the impedance transformer and the antenna radiated power. As a result, the total transistor width is divided into each transistor width according to the load ratio between F_{osc+} and F_{osc-} sides.

The impedance transformation ratio at this particular oscillation amplitude can then be found through the radiated power and the antenna resistance as:

$$P_{rad} = \frac{V_{osc}^2}{2R_{ant-xfmr}} = \frac{V_{osc}^2}{2n^2 R_{ant}}$$

$$n^2 = \frac{V_{osc}^2}{2P_{rad}R_{ant}}. \tag{4.13}$$

The calculated design parameters are summarized in Table 4.1.

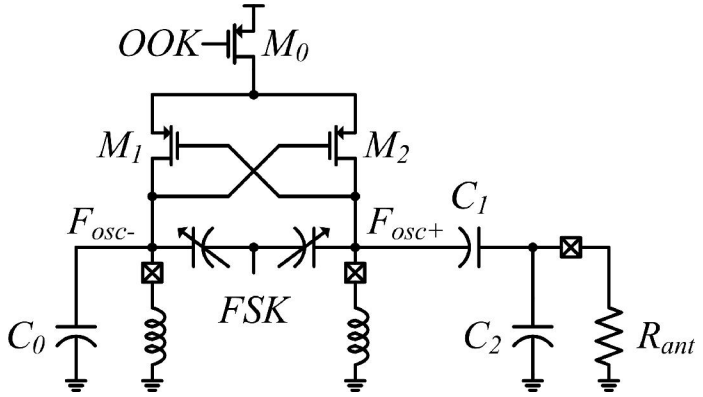

Figure 4.15. Schematic of the prototype power oscillator transmitter.

The implemented transistor width is increased to provide a safety margin. This ensures that the transistor's conductance is high enough to start up the power oscillator even at the corners of process variation. The ratio between the two transistor widths is rounded up into a simple fractional number for accurate layout matching. A similar rounding up is applied to the impedance transformation ratio. The implemented design parameters are given in Table 4.1 for comparison.

Table 4.1. Power oscillator transistor width and impedance transformation ratio.

Design parameters	M_1 width	M_2 width	N^2
Calculation	14.7 μm	71.4 μm	2.56^2
Implementation	16.0 μm	80.0 μm	2.50^2

An additional capacitor, C_0, must be added in the single-ended power oscillator transmitter. It is attached to the oscillation node on the F_{osc-} side which does not connect to the antenna. This capacitor equalizes the capacitance attached on the other side which primarily is the impedance transformer capacitance. Any capacitance

mismatch between these two sides will cause the oscillation amplitude to be attenuated and thus lower the power oscillator efficiency.

The prototype transmitter supports two digital modulation schemes—on-off keying (OOK) and frequency shift keying (FSK). The OOK modulation is achieved with the M_0 transistor at the top of the power oscillator. It acts as an on-off switch for the OOK modulation. Moreover, by dividing the M_0 transistor into multiple small transistors and controlling only a portion of them, the M_0 transistor effectively behaves as a variable resistor. This partial control decreases the effective supply voltage and lowers the radiated power of the power oscillator with a small efficiency degradation. The ability to reduce the radiated power helps reduce the energy consumption when the transmitter communicates at shorter distances than the maximum possible. FSK modulation is accomplished by altering the oscillation frequency through the varactor capacitances.

B. Low-voltage frequency divider

To tune the oscillation frequency, the oscillator output must be compared to a reference signal. Since the reference frequency is usually low, a frequency divider is used to lower the oscillator frequency so that the comparison can be made. A flip-flop-based frequency divider is employed here to minimize the power consumption. The frequency divider in Figure 4.16(a), consisting of a series of divide-by-2 circuits, is the most popular divider structure. However, the output of the first flip-flop can not toggle beyond a GHz with a 0.65 V supply. To overcome this problem, the two

divide-by-2s are combined together as shown in Figure 4.16(b). The input of the two flip-flops is driven by the oscillator output and the output of both flip-flops toggles at a fourth of the oscillation frequency. These two outputs are separated by one period of the oscillation frequency. This creates a divide-by-4 circuit that avoids the flip-flop output toggling at half of the oscillation frequency.

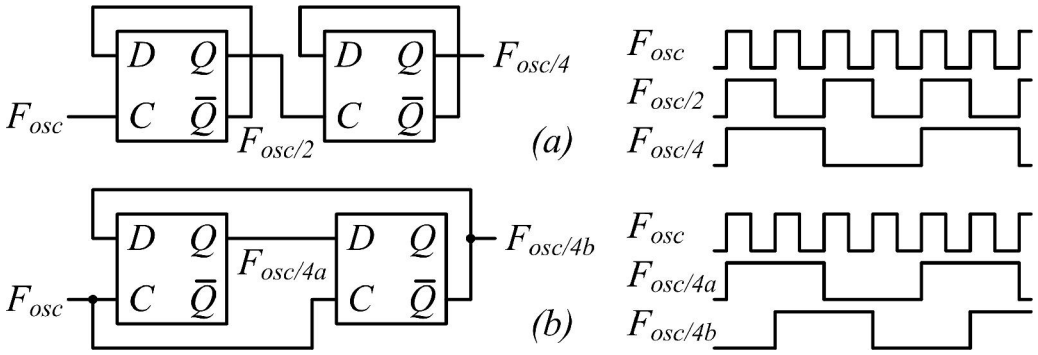

Figure 4.16. Flip-flop-based frequency divider and their timing diagrams. (a) A series of divide-by-2. (b) Divide-by-4.

Figure 4.17(a) shows the flip-flop implementation using the extended-true-single-phase-clocking (E-TSPC) technique [53]. The TSPC technique originally consists of three transistors per branch. The E-TSPC technique eliminates one transistor to increase the speed. The penalty of the transistor elimination is the momentary short-circuit current. Thus, the frequency divider power consumption is increased. However, with a supply voltage as low as 0.65 V, the incremental power consumption is minimal. To further extend the speed, the bulk terminal of the transistors in these flip-flops is forward biased to reduce the transistor's threshold voltage. To interface between the power oscillator and the frequency divider, the

level shifter depicted in Figure 4.17(b) is utilized. Its input is connected to the oscillation node on the F_{osc-} side of the power oscillator and the oscillation DC voltage is shifted to half of the supply voltage at the input of the divide-by-4 circuit.

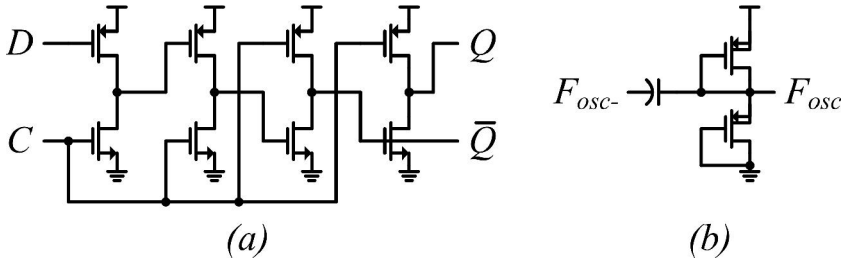

Figure 4.17. Schematics of (a) E-TSPC flip-flop, and (b) its level shifter.

C. Frequency controller

Figure 4.18 displays the frequency controller block diagram [7]. The divided oscillation frequency is an input to the frequency counter. Two numbers of the counter are latched separated by one period of the reference signal (F_{ref}). The difference between these two numbers indicates the oscillation frequency relative to the reference frequency. This is then compared with the desired number (N_{osc}). After that, the varactor controller reads the comparator output and adjusts the oscillation frequency. Finally, two values of the varactor control number which correspond to two oscillation frequencies are kept for BFSK modulation. The frequency counter is realized by TSPC flip-flops connected as a ripple counter. The rest of the frequency controller is synthesized through logic-gate standard cells.

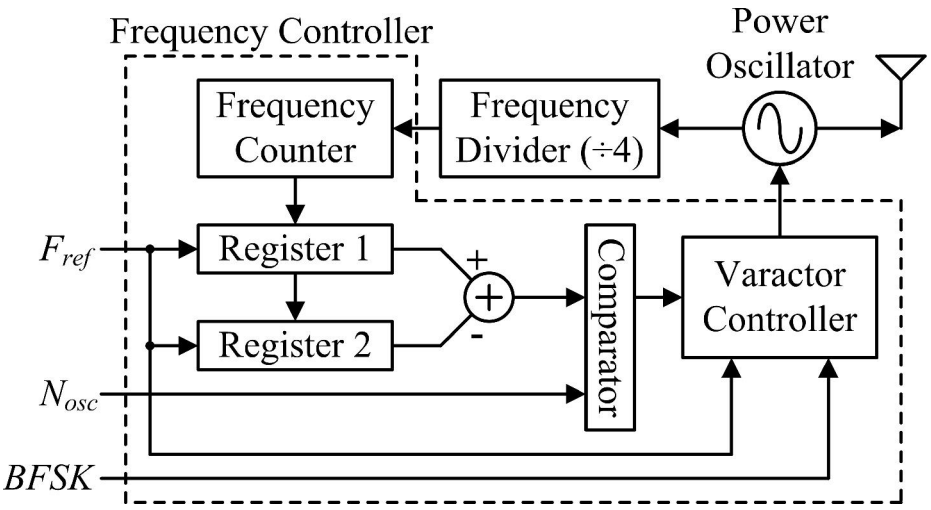

Figure 4.18. Block diagram of the frequency controller.

4.6 Measurement Results

The prototype power oscillator transmitter was fabricated in a 0.18-μm CMOS process. Figure 4.19 shows the die photograph of the transmitter which occupies a small area of 0.89 x 0.64 mm^2. Table 4.2 compares the power oscillator efficiency from calculation, simulation, and measurement. The calculated, simulated, and measured efficiencies are 33 %, 30 %, and 27 %, respectively. The simulated efficiency is lower than the calculated efficiency due to two factors. First, the implemented design parameters were modified from the calculation. Second, parasitic losses due to interconnections between the power oscillator components were not accounted for in the calculation. The measured efficiency is also lower than the simulated efficiency because of the parasitic losses of the chip package and PCB routing which directly reduce the radiated power.

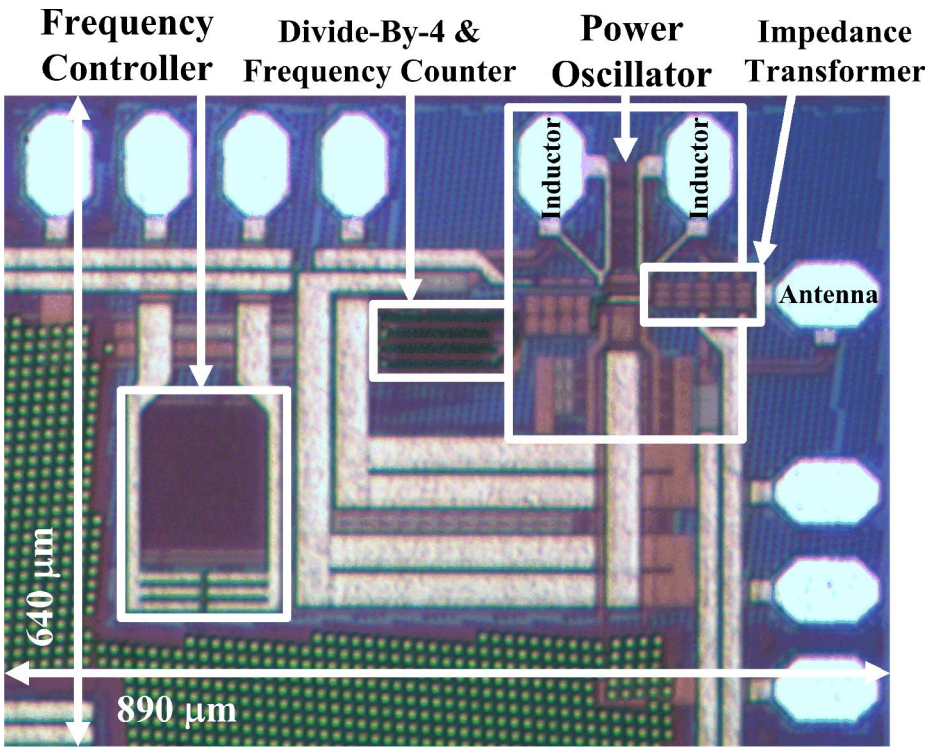

Figure 4.19. Die photograph of the transmitter.

Table 4.2. Comparison of power oscillator efficiency from calculation, simulation, and measurement.

Power oscillator	Calculation	Simulation	Measurement
Oscillation amplitude	0.48 V	0.45 V	-
Radiated power	-4.4 dBm	-4.7 dBm	-5.2 dBm
Efficiency	33 %	30 %	27 %

To verify that the power oscillator design has the maximum efficiency, ideally the transistor's width should be varied. Since the transistor width is a physical dimension and cannot be changed, the supply voltage is varied instead. Figure 4.20 shows the power oscillator efficiency and the output power as the supply voltage

changes from 0.55 to 0.75 V. The higher supply voltage always results in a higher radiated power. However, the power oscillator efficiency decreases as the supply voltage deviates from 0.65 V because the power oscillator is not optimized for the other supply voltages.

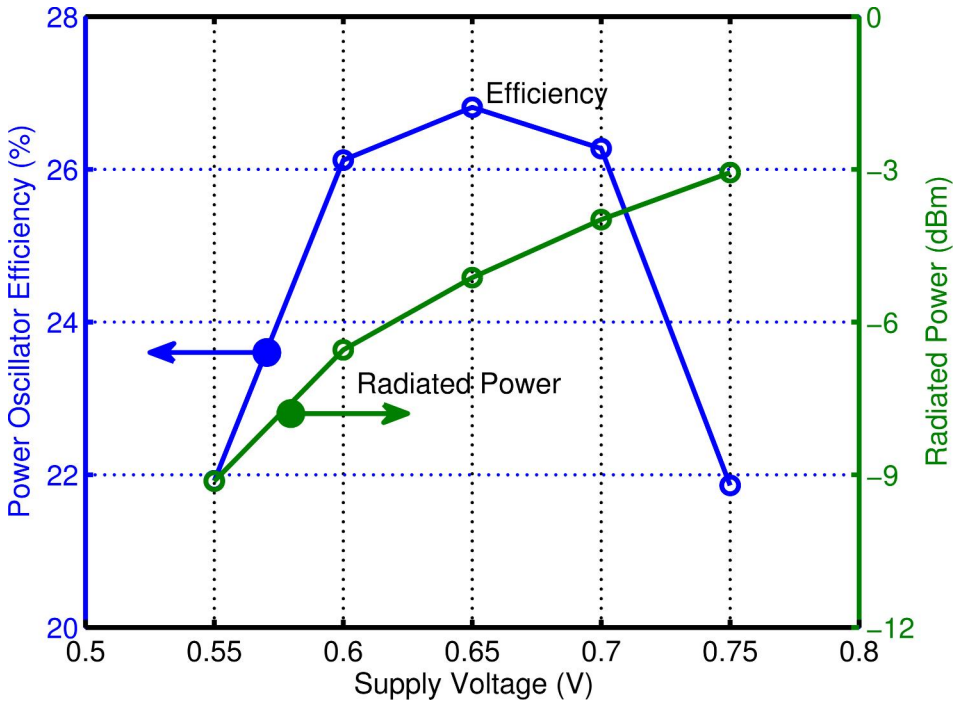

Figure 4.20. Measured power oscillator efficiency and radiated power vs. supply voltage.

Figure 4.21 depicts the power oscillator efficiency as the radiated power is lowered by partial control of the M_0 transistor. The efficiency decreases from 27 % at a radiated power of -5.2 dBm to 18 % at -9.7 dBm. Although the efficiency drops at a lower radiated power, the power consumption also decreases. As a result, the transmitter power consumption can be minimized when the actual communication distance is shorter than its maximum by lowering the radiated power.

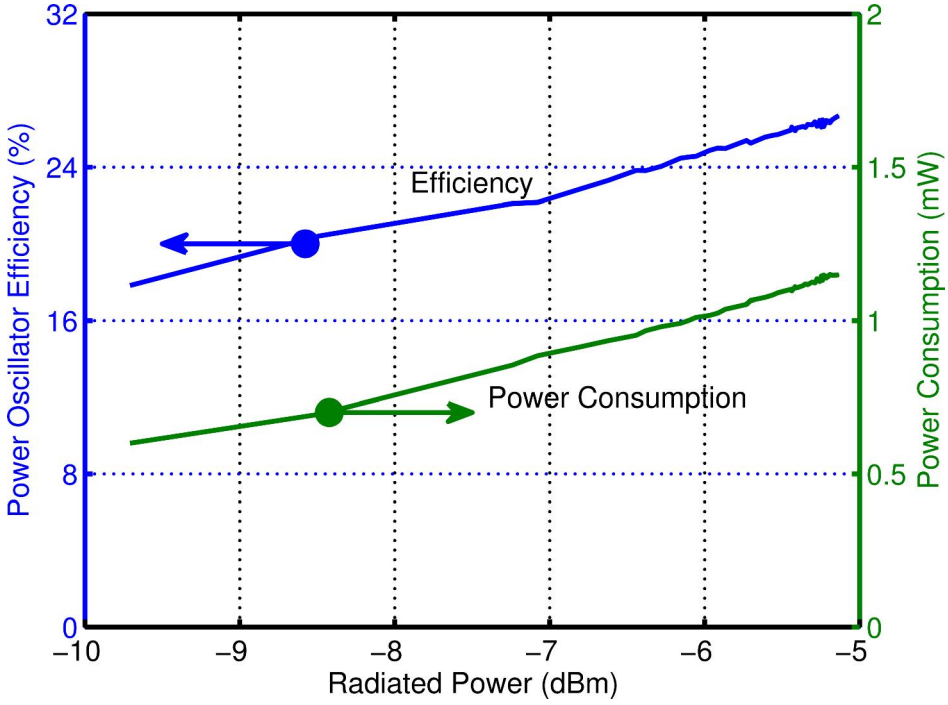

Figure 4.21. Measured power oscillator efficiency and power consumption vs. radiated power.

The oscillation frequency and frequency resolution are plotted in Figure 4.22. The oscillation frequency can be varied from 2.23 to 2.52 GHz which gives a tuning range of approximately 300 MHz. This tuning range is about the same as in the design specification but is shifted down by almost 100 MHz. Nevertheless, the frequency shift is within the tolerance margin and the oscillation frequency is able to cover the entire spectrum of the 2.45-GHz ISM band. Two small frequency overlaps exist because the two MSB varactors are slightly trimmed down to prevent the possibility of frequency skipping. The minimum frequency resolution is about 1.1 MHz with the binary-weighted varactors. The measured phase noise of the transmitter output is -117 dBc/Hz at a 1-MHz frequency offset.

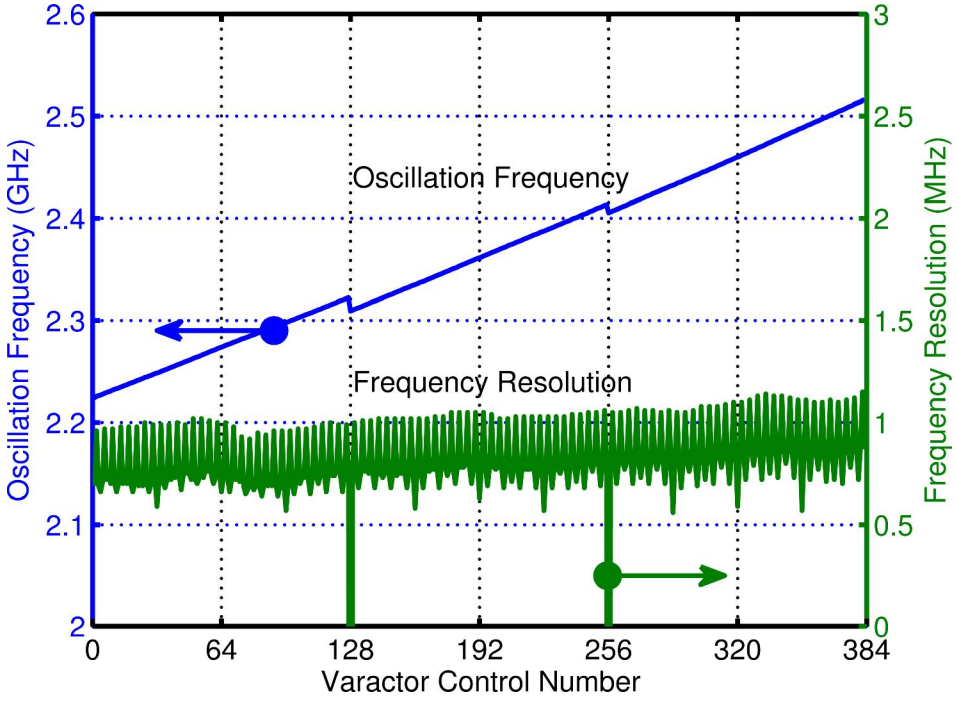

Figure 4.22. Measured oscillation frequency and frequency resolution vs. varactor control number.

Figure 4.23 shows the transient response of the transmitter output when it is turned on and off. The transmitter starts fully oscillating and falls completely idle within 30 and 140 ns, respectively. By assuming that this on-off transition period is 10 % of the OOK bit period, the transmitter is capable of modulating OOK data up to 1.2 Mbps. The frequency divider and the frequency controller combined together have a power consumption of only 0.18 mW. However, the efficiency of the whole transmitter reduces to 23 %. Table 4.3 summarizes the measured results for the prototype power oscillator transmitter.

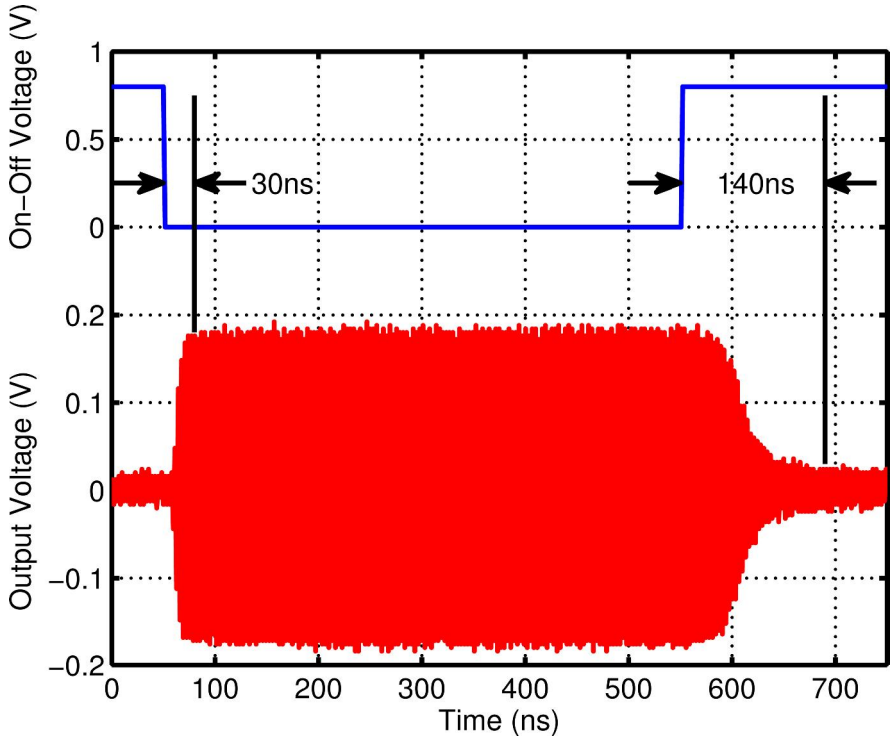

Figure 4.23. Measured output transient with on-off control.

Table 4.3. Performance summary of the prototype power oscillator transmitter.

Technology	0.18-μm CMOS
Supply voltage	0.65 V
Die size	0.57 mm^2
Power consumption • Power oscillator • Frequency divider & controller	 1.15 mW 0.18 mW
Radiated power	-5.2 dBm
Efficiency • Power oscillator • Transmitter	 27 % 23 %
On-off time	30/140 ns

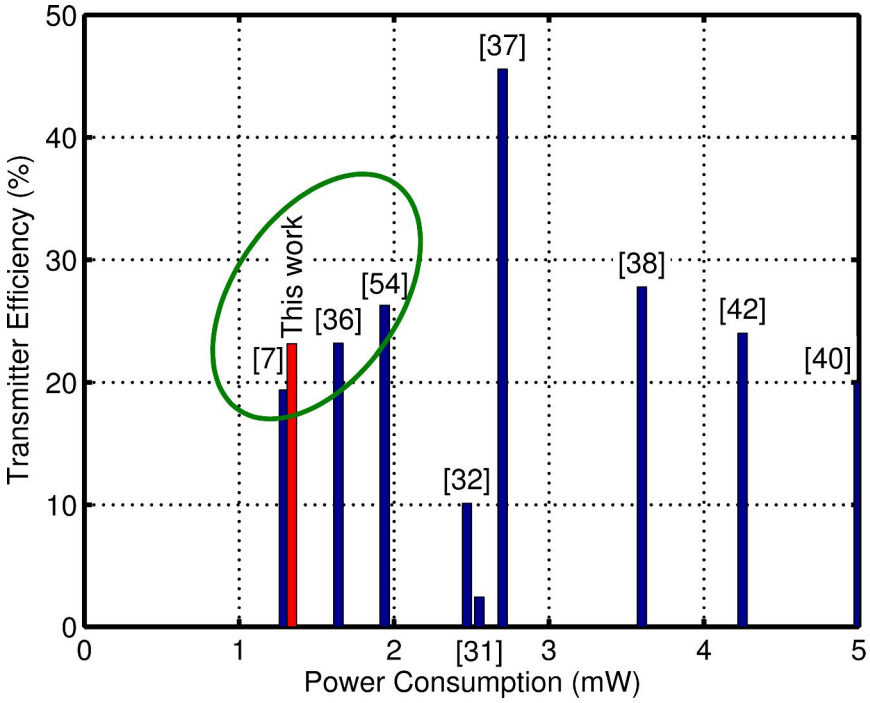

Figure 4.24. Performance comparison of recently published WSN transmitters.

Efficiency and power consumption are generally the two most commonly reported parameters for performance comparison of many circuits. Figure 4.24 plots the transmitter efficiency as a function of the power consumption of the prototype WSN transmitter and recently published WSN transmitters for a performance comparison. The prototype transmitter has higher efficiency than [7] for approximately the same power consumption and has the lowest power consumption compared with other transmitters. A group of WSN transmitters that consume a power less than 2 mW, including this prototype transmitter, is designated by the ellipse. This group of low-power transmitters have a relatively high efficiency of 19 % or higher.

Table 4.4. Key specifications of high-efficiency low-power WSN transmitters.

	[36]	[54]	[7]	[8]	This work
Technology (μm)	0.13	0.18	0.25	0.13	0.18
Supply voltage (V)	1	0.9	0.8[1]	0.4	0.65
Frequency (GHz)	1.9	0.915	0.915	2.45	2.45
Modulation	OOK	BFSK	BFSK	BFSK	BFSK
Power consumption (mW)	1.64	1.94	1.29	1.00[2]	1.34
Radiated power (mW)	0.38	0.51	0.25	0.30	0.31
Efficiency (%)	23	26	19	30[2]	23

[1]With multiple supply voltages (the power amplifier supply voltage is shown).
[2]Without frequency controller.

The key specifications of these high-efficiency low-power transmitters are tabulated in Table 4.4. Table 4.4 also includes the transmitter in [8] which does not implement the frequency controller circuit. A common feature shared among these transmitters is a low supply voltage. This is a critical factor for high efficiency transmitter design particularly for the ultra-low-power WSN transmitters. For example, the supply voltages of three lowest power consuming transmitters are 0.8 [7], 0.65 (this work), and 0.4 V [8] which correspond to 0.25, 0.18, and 0.13 μm technologies, respectively. To achieve the maximum transmitter efficiency, the supply voltage relative to the threshold voltage should be considered as a design parameter. Then, the transmitter efficiency should be evaluated as a function of the supply voltage as demonstrated by this power oscillator transmitter.

The prototype power oscillator transmitter has a fairly high efficiency. It can potentially be employed as a battery-free WSN transmitter by completely supplying the transmitter through an energy harvester. However, the power oscillator efficiency can be further improved by selecting a supply voltage closer to the optimum supply voltage. The optimum supply voltage most likely will be incompatible with the supply voltage of the other circuits. To account for the supply voltage difference, supply management techniques such as current-reused stacking [7] or supply management circuits such as a high-efficiency buck converter [55] must be incorporated. A tradeoff between the increased efficiency and the extra power consumption of the supply management circuitry for the best overall transmitter efficiency must be made.

4.7 Summary

An ultra-low-energy transmitter for wireless sensor networks has been presented. The transmitter based on the power oscillator architecture combines together both the oscillator and the power amplifier for efficient power utilization. The power oscillator is modeled and its efficiency is analyzed mathematically. Following the analysis, a design procedure for maximum power oscillator efficiency is developed. By using the supply voltage as a design parameter, the optimum supply voltage is determined through this design procedure.

The prototype transmitter was fabricated in a 0.18-μm CMOS technology. It operates in the 2.45-GHz ISM band and supports both OOK and FSK modulation

schemes. Operating on a single supply of 0.65 V, the transmitter dissipates a power of 1.34 mW while radiating a power of -5.2 dBm. This corresponds to a relatively high efficiency of 23 %.

5. CONCLUSION

5.1 Conclusion

A wireless sensor network (WSN) consists of a central processing hub and a series of sensor nodes distributed over an area of interest. WSN sensor nodes serve as input terminals, collecting raw data from their physical surroundings. They also act as repeaters, relaying data from one node to the next until it reaches the central processing hub. With this peer-to-peer communication scheme, data can be transmitted over large distances, making a WSN's area of interest highly scalable. Thus, WSNs are ideal for a variety of applications because they can process different types of information and accommodate different parameters of scale. As a result, the demand for WSNs will continue to increase as we move further into the future.

However, few applications currently employ WSNs, as their individual sensor nodes are generally too large, too heavy, and too short-lived to be of use. Designing smaller, lighter, and longer-lasting sensor nodes is therefore an essential step in making WSNs more practical and ubiquitous. In order to reduce the size and increase the lifespan of sensor nodes, their batteries must be eliminated. The key to eliminating a sensor node's battery is minimizing its energy consumption, since high-efficiency sensor nodes can run solely on the power from their energy harvesters. Although several sensor node components require power, sensor node transceivers consume especially high amounts of energy, as they are responsible for the transmission and reception of WSN data. Thus, decreasing the energy

consumption of a sensor node's transceiver is crucial to improving its overall efficiency.

Each sensor node transceiver consists of two parts: a transmitter and a receiver. This dissertation focuses on reducing the energy consumption of WSN transmitters. Many parameters impact transmitter energy consumption, including the number of bits, bit rate, radiated power, start-up time, and transmitter efficiency. Most of these parameters are defined by WSN systems. On the circuit level, the start-up time and the transmitter efficiency are two available parameters for decreasing energy consumption. Minimizing the start-up time limits the energy wasted during a transmitter start-up period. It is especially important to minimize the start-up time of WSN transmitters, as the energy spent during the transmit period is comparatively low. In addition, the transmitter efficiency of WSN sensor nodes must be maximized, since higher transmitter efficiency directly corresponds to lower power consumption for the same radiated power. This dissertation presents two WSN transmitters that have been designed to minimize the start-up time and maximize the transmitter efficiency.

A fast frequency calibration system is employed in the first transmitter to reduce the frequency calibration time, which is the longest period of the start-up time. Fast frequency calibration is accomplished by using a frequency divider with a reset. The reset ability enables the oscillation frequency to be compared within two cycles of the reference frequency. In addition, the frequency divider is implemented with low-power techniques to further minimize the transmitter's energy consumption. This

prototype transmitter operates in the 915-MHz ISM band and is fabricated in a 0.18-μm CMOS process. With a reference frequency of 0.5 MHz, the frequency calibration time of the prototype transmitter is as low as 72 μs for two calibrated frequencies of BFSK modulation. The transmitter outputs -2.9 dBm of radiated power while dissipating 1.91 mW of consumed power and has an efficiency of 27 %.

The second transmitter is designed to maximize the transmitter efficiency at low radiated power levels. The transmitter architecture is based on the power oscillator, which combines an oscillator and a power amplifier in order to minimize transmitter power loss. This dissertation provides a detailed mathematical analysis of the power oscillator efficiency. Then, this efficiency analysis is used to develop a design procedure to maximize the transmitter efficiency for a particular supply voltage. The design procedure is further applied to demonstrate an optimum supply voltage that yields the maximum achievable efficiency. The prototype transmitter is fabricated in a 0.18-μm CMOS process and operates on a single supply of 0.65 V. It communicates in the 2.45-GHz ISM band and achieves a transmitter efficiency of 23 % while radiating a power of -5.2 dBm.

5.2 Future Work

An ultra-low-energy WSN transmitter is developed in this dissertation. Ultra-low-energy WSN transceivers can be implemented by combining this transmitter and the receiver in [14]. This transceiver is capable of communicating with a link energy as low as 0.95 nJ/b [56]. At this level of energy consumption, the transceiver could

sustain itself on a variety of energy harvesters. Therefore, the idea of battery-free WSNs becomes more feasible with this ultra-low-energy WSN transceiver, paving the way for the future of the information age.

Future work includes an investigation of the fundamental limitations for other transmitter architectures. The efficiency for the power oscillator transmitter can be improved by designing the transmitter for an optimum supply voltage. However, this approach requires further research in an efficient power management circuit to generate the desired supply voltage. This power management circuit can be ultimately expanded to efficiently interface all circuits in a sensor node to an energy harvester.

BIBLIOGRAPHY

[1] World Wide Web Consortium, "A little history of the World Wide Web," http://www.w3.org/History.html.

[2] I. F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci, "A survey on sensor networks," *IEEE Communications Magazine*, vol. 40, no. 8, pp. 102-114, Aug. 2002.

[3] Memsic Corporation, "MICA2, TelosB, and IRIS wireless modules," http:// www.memsic.com/wireless-sensor-networks/wireless-modules.html, 2010.

[4] Sentilla Corporation, "Moteiv wireless module," http://www.sentilla.com/ moteiv-transition.html, 2010.

[5] Perpetua Power Source Technologies, "Perpetua Power Pucks," http:// www.perpetuapower.com/products.htm, 2010.

[6] T. T. Le, *Efficient Power Conversion Interface Circuits for Energy Harvesting Applications*, Ph.D. Dissertation, Oregon State University, 2008.

[7] A. Molnar, B. Lu, S. Lanzisera, B. W. Cook, and K. S. J. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *IEEE Custom Integrated Circuits Conference*, Oct. 2004, pp. 401-404.

[8] B. W. Cook, A. Berny, A Molnar, S. Lanzisera, and K. S. J. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757-2766, Dec. 2006.

[9] D. C. Daly and A. P. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1003-1011, May 2007.

[10] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μW wake-up receiver with -72 dBm sensitivity using an uncertain-IF architecture," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 269-280, Jan. 2009.

[11] S. Drago, D. M. W. Leenaerts, F. Sebastiano, L. J. Breems, K. A. A. Makinwa, and B. Nauta, "A 2.4GHz 830pJ/bit duty-cycled wake-up receiver with -82dBm sensitivity for crystal-less wireless sensor nodes," in *IEEE International Solid-State Circuits Conference*, Feb. 2010, pp. 224-225.

[12] J. Chen, M. P. Flynn, and J. P. Hayes, "A fully integrated auto-calibrated super-regenerative receiver in 0.13-μm CMOS" *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1976-1985, Sep. 2007.

[13] J. L. Bohorquez, and A. P. Chandrakasan, and J. L. Dawson, "A 350 μW CMOS MSK transmitter and 400 μW OOK super-regenerative receiver for medical implant communications," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1248-1259, Apr. 2009.

[14] J. Ayers, K. Mayaram, and T. S. Fiez, "An ultralow-power receiver for wireless sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1759-1769, Sep. 2010.

[15] Federal Communications Commission, "The FCC Rules and Regulations," http://wireless.fcc.gov/index.htm?job=rules_and_regulations.

[16] M. Lazarus, "The great spectrum famine," *IEEE Spectrum*, pp.26-31, Oct. 2010.

[17] H. Sheng, P. Orlik, A. M. Haimovich, L. J. Cimini, and J. Zhang, "On the spectral and power requirements for ultra-wideband transmission," in *IEEE International Conference on Communications*, May 2003, pp. 738-742.

[18] J. Ryckaert, M. Verhelst, M. Badaroglu, S. D'Amico, V. D. Heyn, C. Desset, P. Nuzzo, B. V. Poucke, P. Wambacq, A. Baschirotto, W. Dehaene, and G. Van der Plas, "A CMOS ultra-wideband receiver for low data-rate communication," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2515-2527, Nov. 2007.

[19] Y. Zheng, M. A. Arasu, K. Wong, Y. J. The, A. P. H. Suan, D. D. Tran, W. G. Yeoh, and D. Kwong, "A 0.18μm CMOS 802.15.4a UWB transceiver for communication and localization," in *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 118-119.

[20] S. Joo, W. Chen, T. Choi, M. Oh, J. Park, J. Kim, and B. Jung, "A fully integrated 802.15.4a IR-UWB transceiver in 0.13μm CMOS with digital RRC synthesis," in *IEEE International Solid-State Circuits Conference*, Feb. 2010, pp. 228-229.

[21] F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/bit 0.65 V pulsed UWB receiver," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2851-2859, Dec. 2007.

[22] D. Lachartre, B. Denis, D. Morche, L. Ouvry, M. Pezzin, B. Piaget, J. Prouvee, and P. Vincent, "A 1.1nJ/b 802.15.4a-compliant fully integrated UWB transceiver in 0.13μm CMOS," in *IEEE International Solid-State Circuits Conference*, Feb. 2009, pp. 312-313.

[23] M. J. Feuerstein, K. L. Blackard, T. S. Rappaport, S. Y. Seidel, and H. H Xiz, "Path loss, delay spread, and outage models as functions of antenna height for microcellular system design," *IEEE Transactions on Vehicular Technology*, vol. 43, no. 3, pp. 487-498, Aug. 1994.

[24] S. S. Ghassemzadeh, R. Jana, C. W. Rice, W. Turin, and V. Tarokh, "Measurement and modeling of an ultra-wide bandwidth indoor channel," *IEEE Transactions on Communications*, vol. 52, no. 10, pp. 1786-1796, Oct. 2004.

[25] A. Zolfaghari and B. Razavi, "A low-power 2.4-GHz transmitter/receiver CMOS IC," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 176-183, Feb. 2003.

[26] V. Peiris, C. Arm, S. Bories, S. Cserveny, F. Giroud, P. Graber, S. Gyger, E. L. Roux, T. Melly, M. Moser, O. Nys, F. Pengg, P. Pfister, N. Raemy, A. Ribordy, P. Ruedi, D. Ruffieux, L. Sumanen, S. Todeschini, and P. Volet, "A 1V 433/868MHz 25kb/s-FSK 2kb/s-OOK RF transceiver SoC in standard digital 0.18μm CMOS," in *IEEE International Solid-State Circuits Conference*, Feb. 2005, pp. 258-259.

[27] A. C. W. Wong, G. Kathiresan, C. K. T. Chan, O. Eljamaly, O. Omeni, D. McDonagh, A. J. Burdett, and C. Toumazou, "A 1 V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1511-1521, Jul. 2008.

[28] T. Melly, A. Porret, C. C. Enz, and E. A. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: transmitter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 467-472, Mar. 2001.

[29] T. Nguyen, V. Krizhanovskii, J. Lee, S. Han, S. Lee, N. Kim, and C. Pyo, "A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no 12, pp. 4062-4071, Dec. 2006.

[30] H. Seo, Y. Moon, Y. Park, D. Kim, D. Kim, Y. Lee, K. Won, S. Kim, and P. Choi, "A low power fully CMOS integrated RF transceiver IC for wireless sensor networks," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 15, no. 2, pp. 227-231, Feb. 2007.

[31] M. R. Nezhad-Ahmadi, G. Weale, A. El-Agha, D. Griesdorf, G. Tumbush, A. Hollinger, M. Matthey, H. Meiners, and S. Asgaran, "A 2mW 400MHz RF transceiver SoC in 0.18μm CMOS technology for wireless medical applications," in *IEEE Radio Frequency Integrated Circuit Symposium*, Jun. 2008, pp. 285-288.

[32] R. van Langevelde, M. van Elzakker, D. van Goor, H. Termeer, J. Moss, and A. J. Davie, "An ultra-low-power 868/915 MHz RF transceiver for wireless sensor applications," in *IEEE Radio Frequency Integrated Circuit Symposium*, Jun. 2009, pp. 113-116.

[33] F. Carrara and G. Palmisano, "High-Efficiency Reconfigurable RF transmitter for wireless sensor network applications," in *IEEE Radio Frequency Integrated Circuit Symposium*, May 2010, pp. 179-182.

[34] J. P. Carmo, N. S. Dias, H. R. Silva, P. M. Mendes, C. Couto, and J. H. Correia, "A 2.4-GHz low-power/low-voltage wireless plug-and-play module for EEG applications," *IEEE Sensors Journal*, vol. 7, no. 11, pp. 1524-1531, Nov. 2007.

[35] X. Huang, P. Harpe, X. Wang, G. Dolmans, and H. de Groot, "A 0dBm 10Mbps 2.4GHz ultra-low power ASK/OOK transmitter with digital pulse-shaping," in *IEEE Radio Frequency Integrated Circuit Symposium*, May 2010, pp. 263-266.

[36] B. Otis, Y. H. Chee, and J. Rabaey, "A 400μW-RX, 1.6-mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE International Solid-State Circuits Conference*, Feb. 2005, pp. 6-7.

[37] Y. H. Chee, A. M. Niknejad, and J. Rabaey, "A 46% efficient 0.8dBm transmitter for wireless sensor networks," in *Symposium on VLSI Circuits*, Jun. 2006, pp. 43-44.

[38] Y. H. Chee, A. M. Niknejad, and J. M. Rabaey, "An ultra-low-power injection locked transmitter for wireless sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1740-1748, Aug. 2006.

[39] J. Ryu, M. Kim, J. Lee, B. Kim, M. Lee, and S. Nam, "Low power OOK transmitter for wireless capsule endoscope," in *IEEE MTT-S International Microwave Symposium*, Jun. 2007, pp. 855-858.

[40] N. Boom, W. Rens, and J. Crols, "A 5.0mW 0dBm FSK transmitter for 315/433 MHz ISM applications in 0.25μm CMOS," in *European Solid-State Circuits Conference*, Sep. 2004, pp. 199-202.

[41] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, and D. Eggert, "A fully integrated 2.4-GHz IEEE 803.15.4-compliant transceiver for ZigBee™ applications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2767-2775, Dec. 2006.

[42] P. Popplewell, V. Karam, A. Shamim, J. Rogers, L. Roy, and C. Plett, "A 5.2-GHz BFSK transceiver using injection-locking and an on-chip antenna," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 981-990, Apr. 2008.

[43] J. Bae and H. Yoo, "A low energy injection-locked FSK transceiver with frequency-to-amplitude conversion for body-sensor applications," in *Symposium on VLSI Circuits*, Jun. 2010, pp. 133-134.

[44] J. Ayers, K. Mayaram, and T. Fiez, "A 0.4 nJ/b 900MHz CMOS BFSK super-regenerative receiver," in *IEEE Custom Integrated Circuits Conference*, Sep. 2008, pp. 591-594.

[45] T. Oita, "RF MEMS: Focusing on the next step," in *IEEE International Ultrasonics Symposium*, Sep. 2009, pp. 1173 – 1178.

[46] T. Lin and Y. Lai, "An agile VCO frequency calibration technique for a 10-GHz CMOS PLL," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 340-349, Feb. 2007.

[47] W. B. Wilson, U. Moon, K. R. Lakshmikumar, and L. Dai, "A CMOS self-calibrating frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1437-1444, Oct. 2000.

[48] A. Aktas and M. Ismail, "CMOS PLL calibration techniques," *IEEE Circuits and Devices Magazine*, vol. 20, no. 5, pp. 6-11, Sep. 2004.

[49] C. Vaucher and D. Kasperkovitz, "A wide-band tuning system for fully integrated satellite receivers," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 987-997, Jul. 1998.

[50] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039-1045, Jul. 2000.

[51] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 1, pp. 62-70, Feb. 1989.

[52] A. Porret, T. Melly, and C. C. Enz, "Design of high-Q varactors for low-power wireless applications using a standard CMOS process," in *IEEE Custom Integrated Circuits Conference*, Sep. 1999, pp. 641-644.

[53] X. P. Yu, A. Do, W. M. Lim, K. S. Yeo, and J. Ma, "Design and optimization of the extended true single-phase clock-based prescaler," *IEEE Transactions on Microwave Theory and Techniques*, pp. 3828-3835, Nov. 2006.

[54] N. Panitantum, K. Mayaram, and T. S. Fiez, "A 900-MHz low-power transmitter with fast frequency calibration for wireless sensor networks," in *IEEE Custom Integrated Circuits Conference*, Sep. 2008, pp. 595-598.

[55] W. Liou, M. Yeh, and Y. L. Kuo, "A high efficiency dual-mode buck converter IC for portable applications," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 667-677, Mar. 2008.

[56] J. Ayers, N. Panitantum, K. Mayaram, and T. S. Fiez, "A 2.4GHz wireless transceiver with 0.95nJ/b link energy for multi-hop battery-free wireless sensor networks," in *Symposium on VLSI Circuits*, Jun. 2010, pp. 29-30.