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Kai-tuan Kelvin Yan for the degree of Master of Science in Electrical and Computer Engineering presented on Apr. 29, 1992

Title: Wide Bandwidth GaAs MESFET Amplifier

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Leonard Forbes

A high bandwidth operational amplifier has been designed. The cascode configured differential amplifier used in the design resulted in a circuit that is less sensitive to process variation as compared with that of a bootstrapped amplifier design. The circuit contains three differential cascode amplifiers with appropriate level shifters to obtain the optimum DC biasing. The feedback resisitors are source followed to prevent feedforward effects. The uncompensated amplifier has an open loop gain of 6761v/v, a corner frequency of 526MHz, and a unity gain frequency of 9.08GHz. With compensation the corner frequency is improved to 1.15GHz with a compensated phase margin of 65 degree for stability. The above results have been simulated using the professional version of PSpice with process parameters from the TriQuint Semiconductor 1 μm depletion mode technology.

Wide Bandwidth GaAs MESFET Amplifier

By

Kai-tuan Kelvin Yan

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Redacted for Privacy

Head of department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

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Typed by Mun-yuen Wong & Kai-tuan Kelvin Yan for

Kai-tuan Kelvin Yan

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Wide Bandwidth GaAs MESFET Amplifier

1. Introduction

The main motivation behind the work of this thesis is to capitalize on the continuing reduction in the cost of the gallium arsenide GaAs MESFET depletion process so as to design a high bandwidth amplifier. The cascode differential amplifier resulted in a design that is less sensitive to process variations as compared to the bootstrapped amplifier design [1],[2]. The circuit contains three differential cascode amplifiers with appropriate level shifters to obtain the optimum DC biasing. The uncompensated amplifier has an open loop gain of 6761v/v, a corner frequency of 526MHz, and a unity gain frequency of 9.08GHz. With compensation the corner frequency is improved to 1.15GHz with a compensated phase margin of 65 degree for stability. The above results are simulated using the professional version PSpice with process parameters from the TriQuint Semiconductor 1 μm depletion mode technology.

In chapter two, the characteristics of GaAs are studied and contrasted with that of silicon, Si, demonstrating in particular, why the conventionally available GaAs depletion mode MESFET is chosen. Investigation is made as to the various type of models available for GaAs MESFETs and why the Curtice model reflected by level 1 in the PSpice is chosen.

The first part of chapter three investigates the design of a

single stage GaAs amplifier. A cascode differential amplifier with a differential gain of close to 30 is investigated. The high cascode gain is achieved at the expense of the need for level shifters at the inputs. A higher gain amplifer can be obtained by cascading identical the cascode differential amplifier . For stability, the phase margin needs to be around 60 degree, as such compensation is required. A study of the different kinds of compensation techniques has been made. The consequences of employing such techniques in terms of the area requirement and complexity issues are investigated. The final part of chapter three discusses the compensation of the three stage GaAs amplifier .

In chapter four, a comparison between the composite cascode differential amplifier which has been designed with Larson's and Toumazou's GaAs Mesfet operational amplifier circuit designs is performed. To make the comparison credible, all these designs are simulated using the level 1 Curtice model, instead of using the models which are specified in the different papers from which the GaAs operational amplifier circuits are extracted. The proposed design of the GaAs operational amplifier in this thesis is less sensitive to process variations as compared to the other operational amplifier circuits.

2. GaAs MESFET

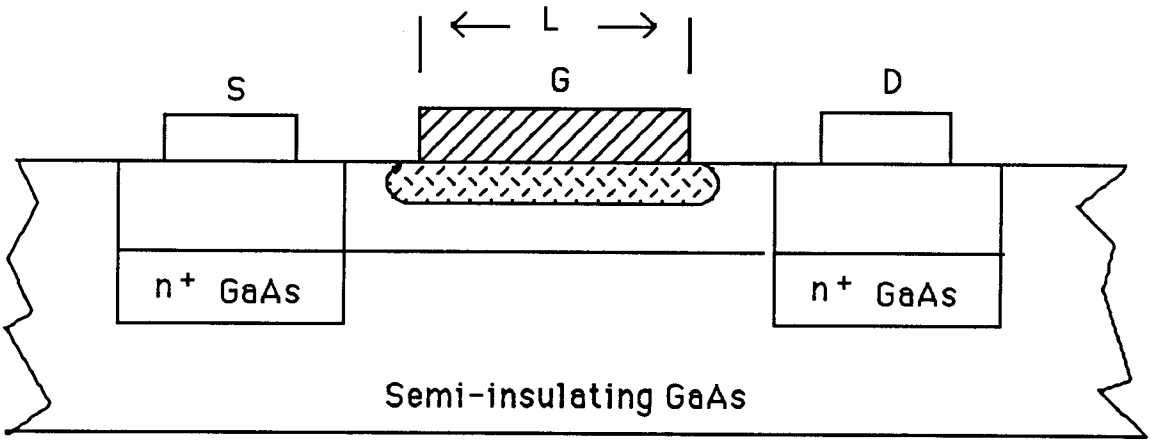
2.1 GaAs versus Si

Some important electronic and material properties of GaAs and Si are illustrated in Table 2.1 for the purpose of comparing the advantages and disadvantages of GaAs MESFET over its Si MOSFET counterpart [3].

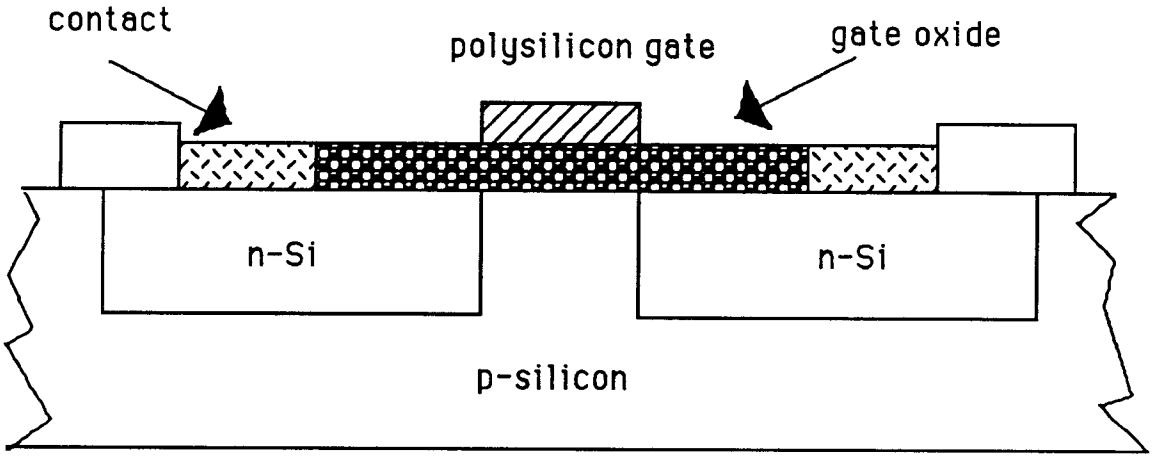
Property	GaAs	Silicon
Bandgap	Direct; 1.42 eV	Indirect; 1.12 eV
Electron drift mobility	5000 $cm^2/V.S$	800 $cm^2/V.S$
Hole drift mobility	250 $cm^2/V.S$	300 $cm^2/V.S$
Substrate resistivity	> 10^6 Ω/cm	> 30 Ω/cm
Native oxide	no	SiO_2

Table 2.1 Critical Properties Comparison Between GaAs & Si

GaAs MESFET versus Si MOSFET.



(a) MESFET



(b) MOSFET

Figure 2.1 Cross-sectional representation of (a) MESFET and (b) MOSFET [3]

The direct band gap property of GaAs is typical of many III-V compound semiconductors and is essential for efficient light emission. This explains the dominance of GaAs in most optoelectronic applications. The direct band gap property of GaAs allows for light emission such that the electron are able to make a transition from the conduction band to the valence band without requiring phonon scattering at the same time [3].

The electron mobility of GaAs is on the average approximately 6 times that of Si which is the main reason for using GaAs in high speed applications.

As indicated in Table 2.1, GaAs has a hole mobility of 250 $cm^2/V.S$. This is lower than Si which has a hole mobility of $300cm^2/V.S$. This disadvantage rules out the possibility of creating a commercially viable p-channel MESFET. The absence of p-channel MESFET's means that GaAs MESFET technology does not have an equivalent Si CMOS implementation. Thus the currently available circuit techniques in CMOS technology cannot be exploited. One critical advantage of CMOS technology is the lower static power consumption that is important in very large scale integration which involve thousands of devices.

Substrate resistivity needs to be sufficiently high to assure acceptable low leakage current between circuit elements. GaAs with a substrate resistivity on the order of 10^6 to 10^8 cm which is very high compared to Si, has an obvious advantage.

A lower parasitic substrate capacitance is obtained with GaAs semi-insulating substrate. Given a same size device, the small

depletion depth of Si in comparison with GaAs, results in a greater parasitics capacitance per unit area [3]. For the same device area, the relatively small depletion depth of Si leads to high capacitance per unit area which results in the greater parasitic capacitance for Si as compared to GaAs. Another advantage of GaAs over Si is its radiation hardness. This is an important property especially in space and military applications.

Si MOSFET technology has a very stable native oxide SiO_2. GaAs on the other hand does not have any. The MESFET structure which make use of metal Schottky contact does not require any native oxide. The SiO_2 oxide in MOSFET's is use to insulate the gate electrode from the device channel which allows a wide range of gate voltages to be used without significant gate conductivity.

2.2 GaAs Models

A model only reflects the approximation of the physical reality of the device and a compromise need to be made between its complexity and accuracy. All models should seek to achieve all the critical device characteristics and yet must be computer time efficient.

Therefore, the suitability of the model depends on the different type of circuits involved. For instance, a model that is used to design microwave amplifiers need to have perfect terminal matching. Therefore the nonlinear model of the MESFET should predict accurately both the small-signal and large-signal terminal

impedances of the device. As such, the model should give an accurate measure of the drain-source conductance whereas accurate values of the channel voltage V_{ds} and channel current I_{ds} are not so important.

It should always be noted that the most parameters required in the model are only approximation from S-parameter and DC I-V curves. The measurements used to produce these curves should be as accurate as possible and should take into account all aspects of measurement setup such as bond wire inductances and pad capacitances etc. Again a compromise between the accuracy of a model and the complexity and computation time involved to predict a model has to be reached.

2.2.1 Curtice Model

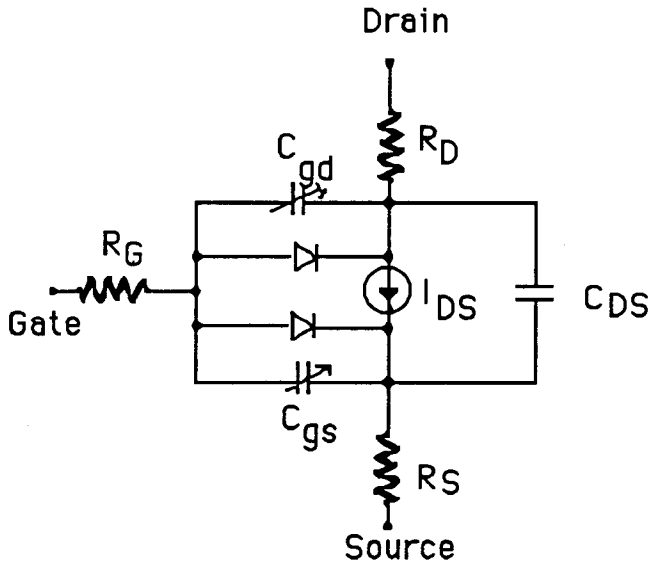


Figure 2.2 PSpice circuit model

The drain current I_d, exclusive of the parasitic resistances can be approximated by

$$I_{ds} = \beta (1+\lambda V_{ds}) (V_{gs} - V_t)^2 \tanh (\alpha V_{ds})$$

In the above equation, V_{gs} is the gate to source voltage, V_{ds} is the drain-to-source voltage, V_t is the threshold voltage, ß is a parameter, Lamda is a parameter related to the drain conductance, and determines the voltage at which the device saturate. Curtice [4] uses the same equation to estimate the drain current for the linear and the saturation region. Therefore I_{ds} saturates at the

same V_{ds} irrespective of the gate-to-source voltage V_{gs}. This model does not reflect very accurately the variation of I_{ds} with the changing value of Vgs especially if the V_t is large.

This model is adopted as the level 1 GaAs MESFET model in PSpice. It should be noted that there also exists a Curtice cubic model which takes into consideration the power relationship between I_{ds} and V_{gs} and the saturation voltage control to stimulate the negative conductance of the dipole which forms at the drain end of the channel [5]. These additional parameters of the Curtice cubic model are meant to improve the accuracy and account for second order effects. The complicated formulae resulting and difficulty of making model parameter indentifications does not make it feasible for use in PSpice.

2.2.2 Statz Model

The level 2 GaAs MESFET model in PSpice or the Statz model [6] gives good accuracy for simulation of the channel current of the MESFETs because it is a model which predicts accurately saturation velocity of GaAs in both the linear and saturation region.

$$I_{ds} = \frac{\beta\ (V_{gs} - V_t)^2}{1 + B\,(V_{gs} - V_t)}\ (1 + \lambda V_{ds})\tanh(\alpha V_{ds})$$

B has a value between 2.6 V^{-1} and 1.5 V^{-1} and is a measure of the doping profile extending into the semi insulating substrate and thus dependent on the fabrication process.

To better approximate the saturation velocity of GaAs, the term $\tanh(\lambda V_{ds})$ or $\tanh(x)$ is introduced as follows:

$$0 < x < 3 \quad \text{(linear region)}$$

$$\tanh(x) = 1 - \left(1 - \frac{x}{3}\right)^3$$

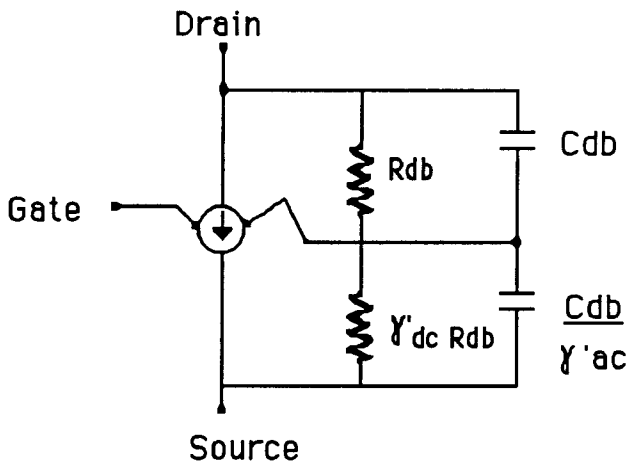
$$x > 3 \quad \text{(saturation region)}$$

$$\tanh(x) = 1$$

For both PSpice level 1 and 2, the tanh(x) function consumes considerable computer time and thus it is approximated by a simple polynomial P,

$$P = 1 - \left(1 - \frac{\lambda V_{ds}}{n}\right)^n \quad \text{with } n = 3$$

2.2.3 TriQuint own model



$$\gamma' = \frac{\gamma}{1-\gamma}$$

Figure 2.3 TriQuint own model

The above model is a recently released model by TriQuint Semiconductor [9]. It sought to rectify some disadvantage of the Statz Model. The Statz Model previously discussed fails to provide an accurate model at low currents where the V_{gs} is near the cutoff. As such this will lead to an erroneous prediction of small-signal parameters such as gain and drain resistance over the dynamic range of the device. The Statz expression for drain current is used

$$I_{dso} = \frac{\beta\ (V_{gs} - V_t)^2}{1 + B\,(V_{gs} - V_t)}\ (1 + \lambda\ V_{ds})\tanh(\alpha V_{ds})$$

The first modification is to have a better drain conductance fit at low drain current. This is done by modifying the V_t in the Statz I_{ds} equation as such

$$Vt = V_{to} - \gamma V_{ds}$$

The second modification is to emphasize the way I_{ds} decreases at higher values of current and voltage. This model also take into consideration the non-square-law dependence of I_{ds} which is observed for devices with small or positive pinch off voltages.

$$I_{ds} = \frac{I_{dso}}{1 + \delta\ V_{ds}\ I_{dso}}$$

The new parameters δ and γ replace λ and B in the Statz model.

2.2.4 Tajima Model

The above model [7] [8] is very suitable for microwave applications as it provides an excellent fit to the DC I-V characteristic curve.

$$I_{ds}(V_{ds}, V_{gs}) = I_{d1} \cdot I_{d2}$$

$$I_{d1} = \frac{1}{k}\left[1 + \frac{V'_{gs}}{V_p} - \frac{1}{m} + \frac{1}{m} \exp\left\{ -m\left(1 + \frac{V'_{gs}}{V_p} \right) \right\} \right]$$

$$I_{d2} = I_{dsp}\left[1 - \exp\left\{ \frac{-V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}} \right)^2 - b\left(\frac{V_{ds}}{V_p} \right)^3 \right\} \right]$$

$$k = 1 - \frac{1}{m}\{ 1 - \exp(-m) \}$$

$$V_p = V_{po} + pV_{ds} + V_\phi$$

$$V'_{gs} = V_{gs} - V_\phi$$

The parameters a, b, m, and P are the fitting factors.

V_{po} (>0) : the pinch off voltage at $V_{ds} \sim 0$

V_{ds} : drain-to-source saturation voltage

$V_ø$: the built-in potential of the Schottky barrier

I_{dsp} : drain current when $V_{gs}=V_ø$

This model is purely empirical. Since it is not based on physical properties, the parameters are extremely difficult to extract. Therefore, the use of the above model for the general purpose PSpice program is doomed to be impractical.

2.2.5 Materka model

The Materka model [9] [10] uses a very simple formulae to describe the DC-IV characteristics.

$$I_{ds}(V_{gs}, V_{ds}) = I_{dss}\left(1 + \frac{V_{gs}}{V_t}\right)^2 \tanh\left(\frac{\alpha V_d}{V_{gs} + V_t}\right)$$

V_t = V_{to} + V_d

I_{dss} = saturation current

V_{to} = effective threshold voltage

α, and γ are parameters of the model

The above model is a simplified version of the Tajima model discussed earlier. Instead of 4 parameters used in the Tajima model, the Materka model has only 2 parameters.

2.2.6 Larson Model

Another recent model used by the group from Hughes Aircraft is the Larson's model [1].

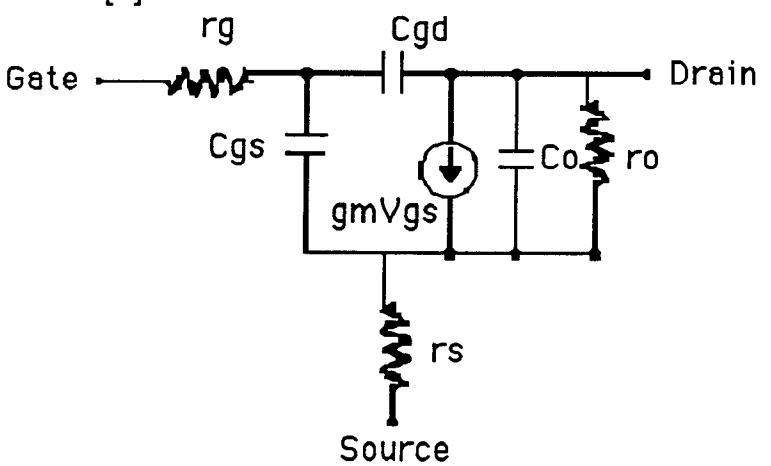


Figure 2.4 Larson circuit model

The empirical equation for the Ids for this model is not in the literature. The model is extracted from the publication which presented the design of an ultra high-speed GaAs MESFET operational amplifier.

2.3 Conclusion

In any integrated circuit design, a computer simulated result is sought first. But prior to choosing the best suitable model available in the literature for the purpose of predicting the behavior of a circuit, we are constrained by the simulation tool on hand. The current version of the PSpice available support only the Curtice model level 1 and the Statz model level 2 modelling. Other computing resources such as the Mentor Graphic tools do not support the GaAs MESFET models. As such we are limited to choosing between either the Curtice or the Statz model. The simple Curtice model is selected in view of the that the circuit designed is not targeted for used in large-signal microwave applications and our process parameters chosen from TriQuint Semiconductor has a reasonable pinch off voltage of -1.5V.

3. GaAs MESFET Operational Amplifier

This chapter illustrates the step by step design of a GaAs MESFET operational amplifier. During the progress of the design, several variations of the circuit design are discussed with the sole purpose of highlighting the advantages as well as limitations of the final design. The most important criterion for design is the wide bandwidth. With this in mind the final circuit is constructed. Wide bandwidth amplifiers find application in satellite communications and high speed communication systems.

3.1 Single stage cascode differential amplifier

3.1.1 Circuit Description

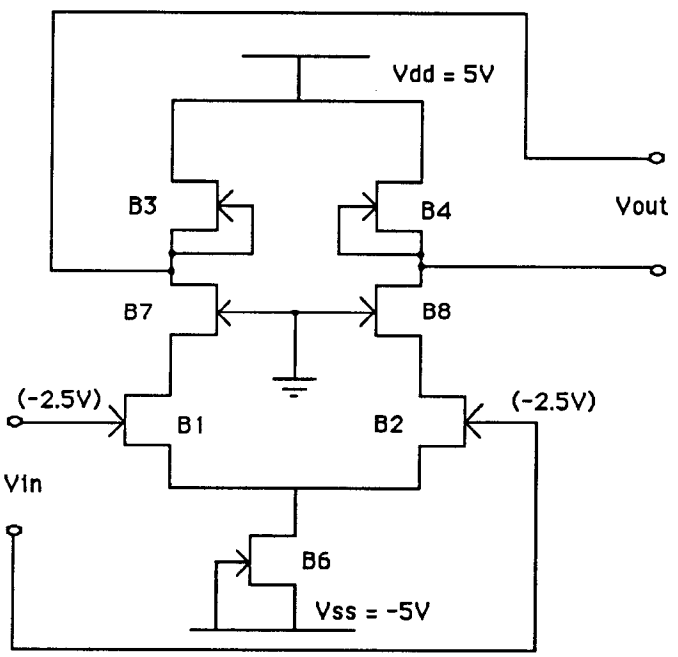


Figure 3.1 Single stage cascode differential amplifier

With the Curtice Model chosen as the model for the simulation, the gm and gd for the MESFET can be calculated by:

$$I_{ds} = \beta (1+\lambda V_{ds}) (V_{gs} - V_t)^2 \tanh (\alpha V_{ds})$$

$$gm = \frac{d I_{ds}}{d V_{gs}} = 2 \beta (1+\lambda V_{ds}) (V_{gs} - V_t) \tanh (\alpha V_{ds})$$

$$gd = \frac{d I_{ds}}{d V_{ds}}$$

$$= \beta (V_{gs} - V_t)^2 [(\alpha+\lambda\alpha V_{ds}) \operatorname{sech}^2 (\alpha V_{ds}) + \lambda \tanh (\alpha V_{ds})]$$

GaAs MESFET		
Model parameter	Value	units
V_{to}	-1.5	Volt
V_{B1}	0.8	Volt
ALPHA	2	1/(volt)
Beta	0.07	amp/volt^2
Lambda	0.05	1/(volt)
R_S	1	ohm
R_D	1	ohm
CGD	0.5	pico-farads
CGS	0.5	pico-farads

Table 3.1 TriQuint GaAs MESFET L=1μm and W=1000μm depletion mode process parameters

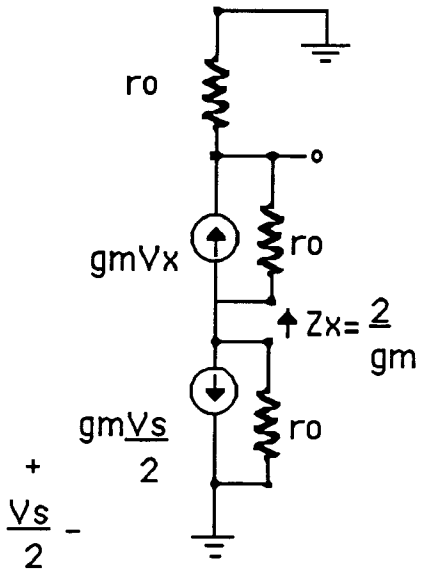


Figure 3.2 AC equivalent half circuit of the cascode differential amplifier

$$A_{v1} = gmZx$$

$$= gm\left(\frac{2}{gm}\right) = 2$$

$$A_{v2} = gmRl$$

$$\text{but } Rl = r_o \,\backslash\backslash\, r_o = \frac{r_o}{2}$$

$$A_{v2} = \frac{gmr_o}{2}$$

$$\text{Total } A_v = A_{v1}\, A_{v2}$$

$$= -gmr_o$$

$$\text{But } r_o = \frac{1}{gd}$$

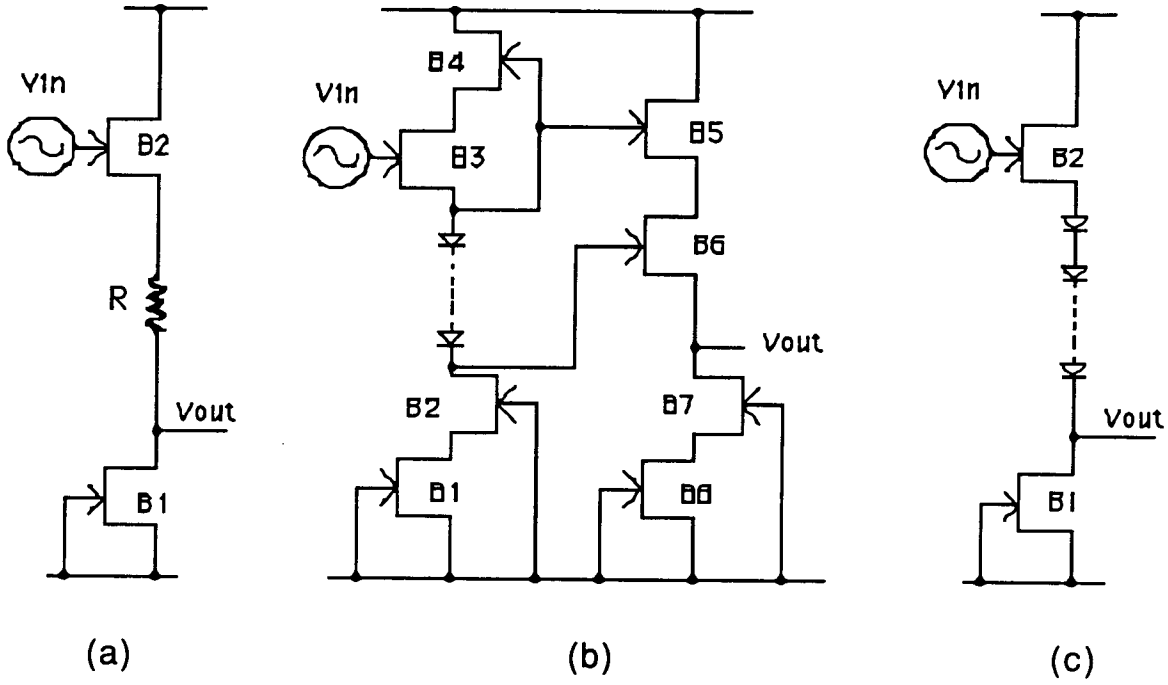
$$A_v = \frac{-gm}{gd}$$

Av is the gain of the differential amplifier taken single ended. This means that the differential gain is equal to -2Av or -2gm/gd. The presence of B7 and B8 of Figure 3.1 provides the necessary cascoding. Without these the overall gain would be reduced by half.

The length of all devices is maintained constant at 1μm and only the width is changed. For B1, B2, B3, B4, B7,and B8 the widths are equal to 20μm and the current source configured MESFET B6 has a width of 40μm. With the rail voltages at +5V and -5V, to achieve a proper DC biasing voltage of V_{GS}= -2.5V, the input to the amplifier has to be level shifted to -2.5V. This necessitates the need for level shifters at the inputs.

3.1.2 Level shifters

To match the DC bias of -2.5V at the input, the Vin has to level shifted from DC 0V to DC -2.5V. The possible level shifters from the literature are:



(a) (b) (c)

Figure 3.3 Different Level Shifters

Figure 3.3(a) which has the requirement of a resistor R, needs considerably more area than the diode configured MESFET of Figure 3.3(c).

Figure 3.3(b) has the advantage that the gain is better than Figure 3.3(c), its gain is very close to 1. However, the complexity of the circuit necessitates the use of more devices and thus higher overall parasitic capacitances which also means a reduction of bandwidth.

Figure 3.3(c) has the best fit for our specification of wide bandwidth requirement. The diode in this circuit can be constructed using only regular MESFETs with the drain and gate connected. The circuit has a simulated gain of approximately 0.81.

Therefore, Figure 3.3(c) is selected for the level shifters for the present single stage amplifier as well as any later two stage or three stage design.

Thus the design of the single stage amplifiers is as follows:

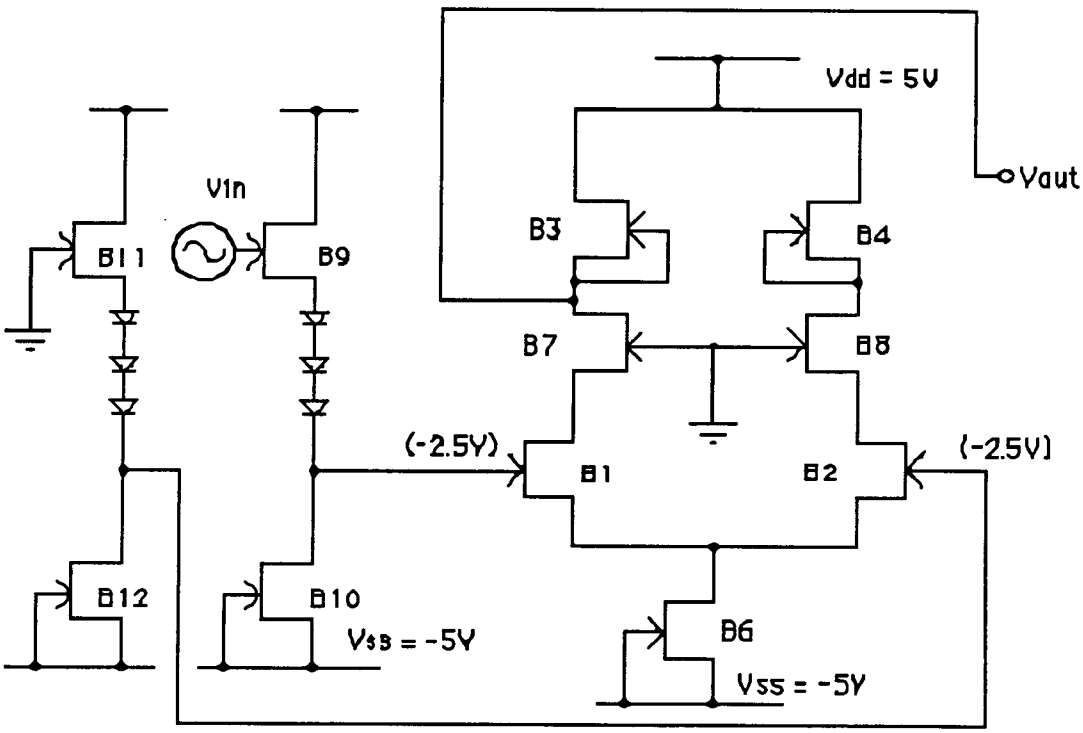


Figure 3.4 Complete design of a single stage amplifier

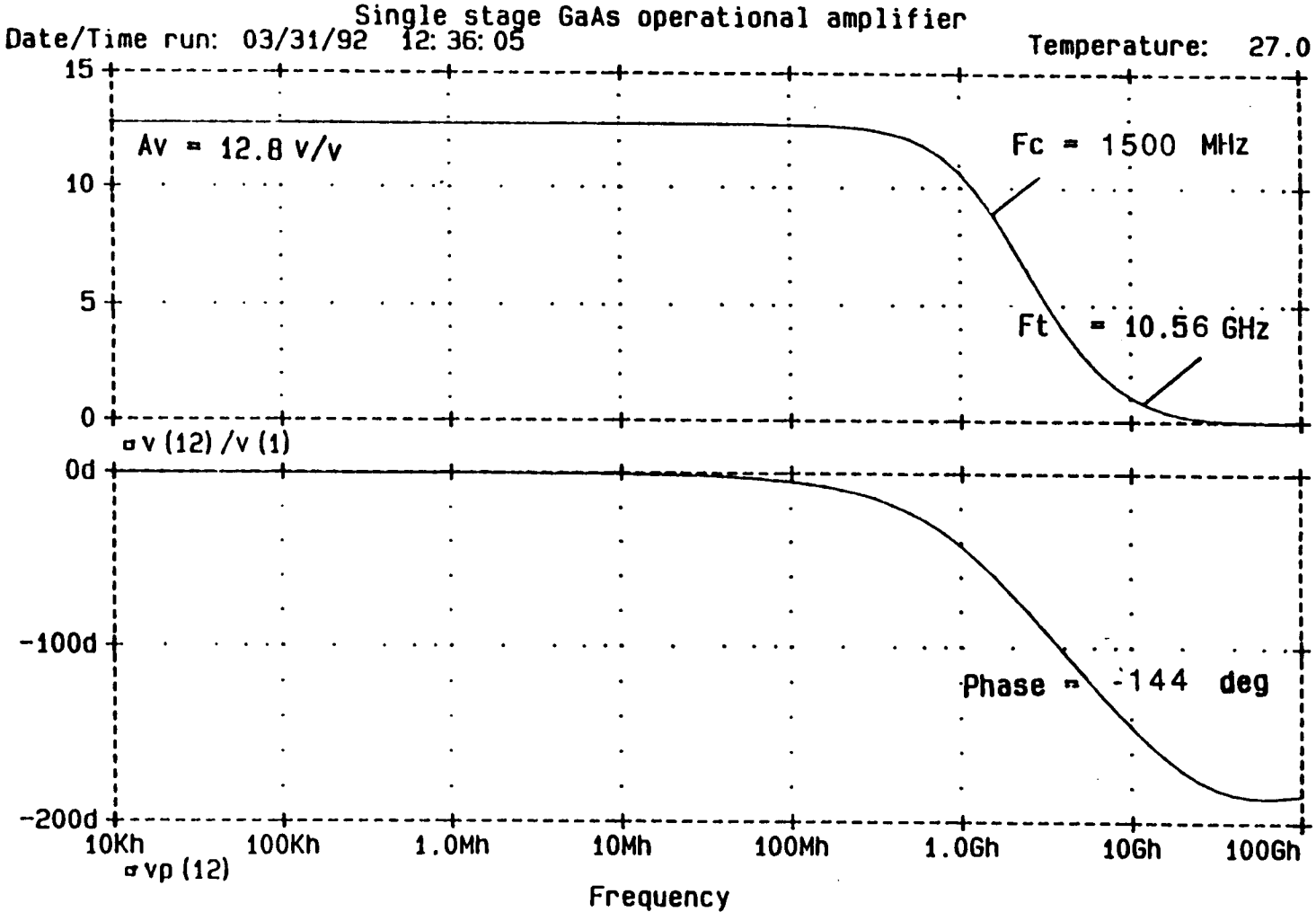
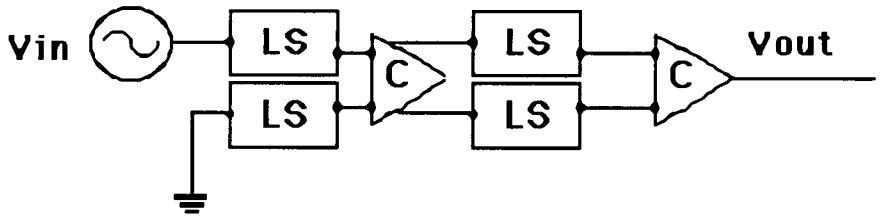


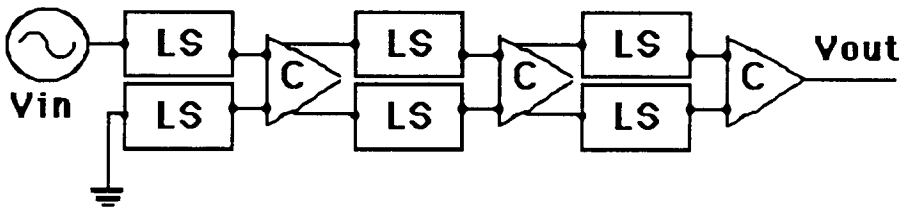
Figure 3.5 Single stage cascode differential amplifier gain & phase plot

3.2 Improvement of the gain



C : Cascode differential amplifier
LS : Level Shifters

Figure 3.6 Two Stage GaAs MESFET Operational Amplifier



C : Cascode differential amplifier
LS : Level Shifters

Figure 3.7 Three Stage GaAs MESFET Operational Amplifier

The gain of the amplifier can be increased by cascading the single cascode differential amplifiers. It should be noted that the output of the cascode amplifier have a DC bias of +2.5V which needs to be level shifted to DC -2.5V before being fed into the input of the next stage which is again a cascode differential amplifier. These can be done as shown in the block diagram in Figure 3.5 and Figure 3.6.

	Single	Two Stage	Three Stage
DC open loop gain (v/v)	12.8	319	7765
Unit gain frequency (GHz)	10.59	10.59	10.59
Bandwidth (MHz)	1500	780	577
Phase angle (degree)	-140	-309	-470
Power Consumption (mW)	115	229	343

Table 3.2 Single, Two and Three Stages Simulation results

Therefore a two stage and three stage amplifier can be constructed in this way and the results are simulated and compared in Table 3.2. We observe that by increasing the number of cascode stages, the gain of the amplifier can be increased significantly. However, the phase margin will also be worse and become intolerable which means the circuits for the two and three stage amplifier are unstable. This necessitate the presence of compensation to make the phase margin approximately between 45 to 60 degree for stability. Phase margin is a measure of deviation from the phase angle of -180 degree.

3.3 Output Stage

3.3.1 Class A Output Stage

The output stage chosen for our design is a simple class A output step [12] [13]. The source follower action of the output stage serves to lower the output impedance. Since the amplifier is designed mainly for high frequency use, the output impedance is

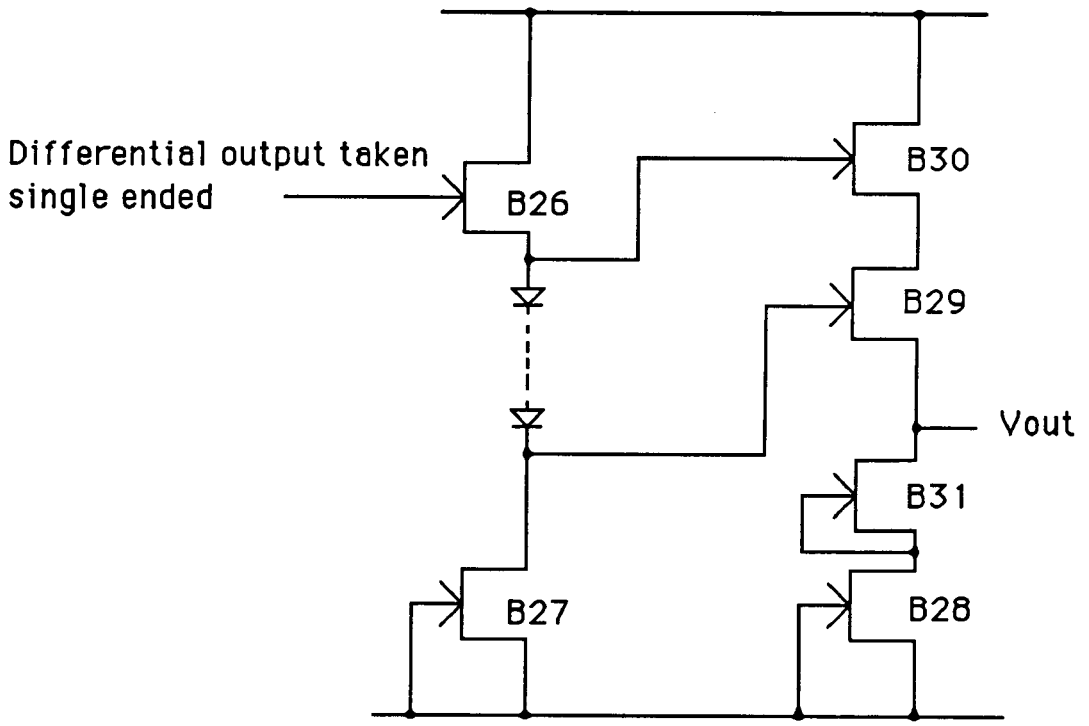


Figure 3.8 Class A Output Stage

adjusted to be as close to 50 ohm as possible. This reduction in the output impedance is achieved by increasing the size of the stage transistors, B28, B29, B30 and B31.

The presence of the level shifter represented by B26 and B27 is to try achieve zero offset set voltage at the output. The transistor B31 is present to achieve symmetry at the output as well as to maintain reasonable biasing of the transistors. Two identical current source transistors B31 and B28 contribute to minimizing matching problems. Since the transistor size of B28 and B31 is large, the mismatch is less prominent. A limitation of the Class A output stage is that the power consumption is higher when compared to a Class AB output stage design.

3.3.2 Class AB Output Stage

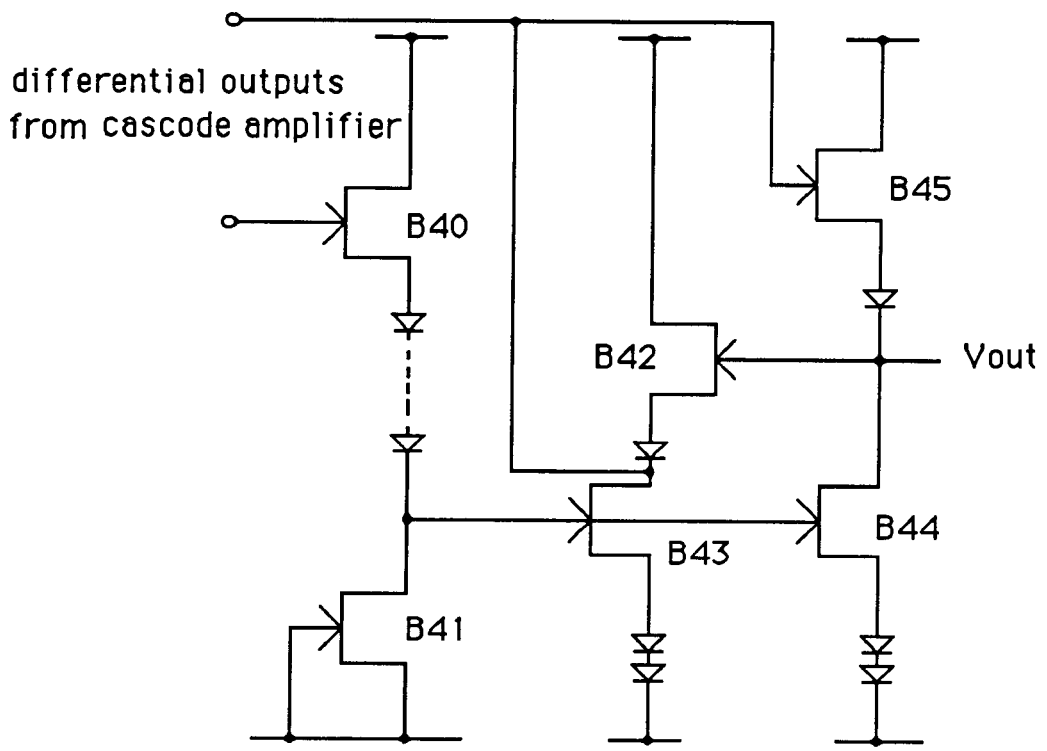


Figure 3.9 Class AB Output Stage

Figure 3.9 shows the design of a Class AB output stage by Taylor [14]. The Class AB action is aimed at minimizing the cross over distortion as well as the power dissipation. The above design is also aimed at making the bias current in the output device more easily controlled.

This Class AB output stage requires the use of an additional level shifter represented by B40 and B41 which will deteriorate the bandwidth of the operational amplifier.

3.4 Maximization of Bandwidth

3.4.1 Level Shifter Compensation

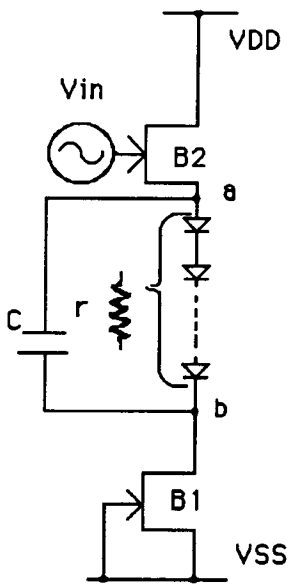


Figure 3.10 Level Shifter capacitive compensation [15]

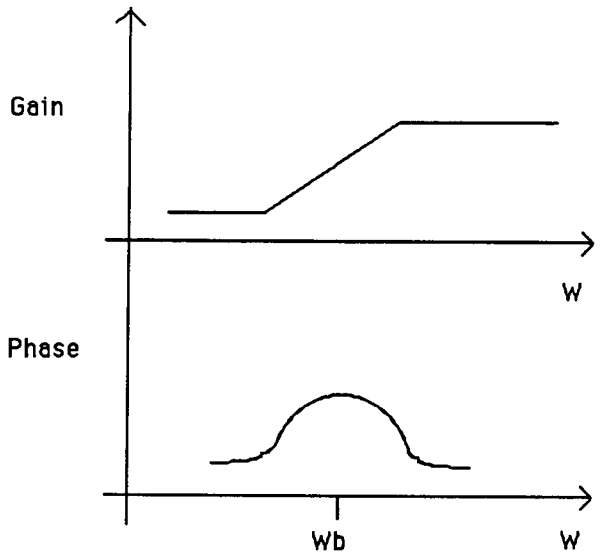


Figure 3.11 Impact of Level Shifter capacitive compensation in the phase plot

For the MESFET configured diode, let r denote the total series resistance from a to b. With a chosen value Wb and r, the compensating capacitor C, can be computed via:

$$w_b = \frac{1}{r\,C}$$

$$C = \frac{1}{w_b r}$$

Depending on the range of frequency where compensation is most needed the phase margin can be subsequently improved.

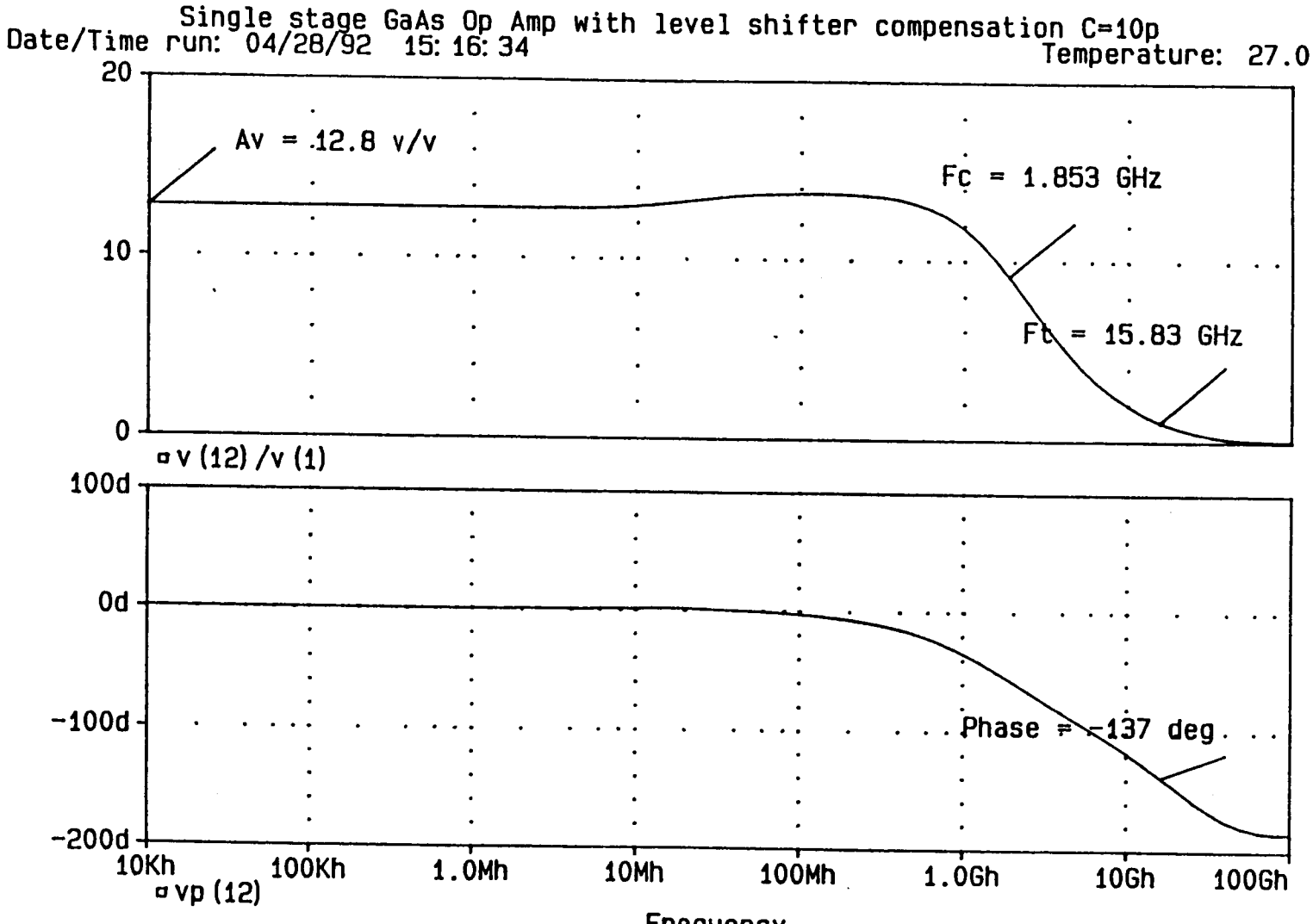


Figure 3.12 Single stage cascode differential amplifier with capacitive compensation gain & phase plot

3.4.2 Inductive Frequency Compensation

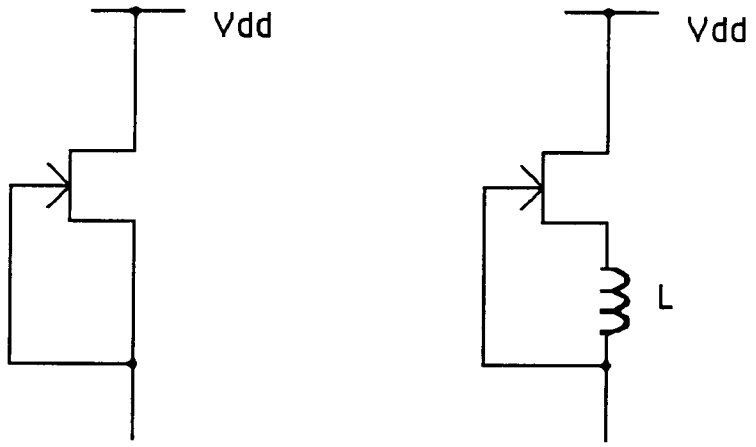


Figure 3.13 Compensation by embedded inductor [16]

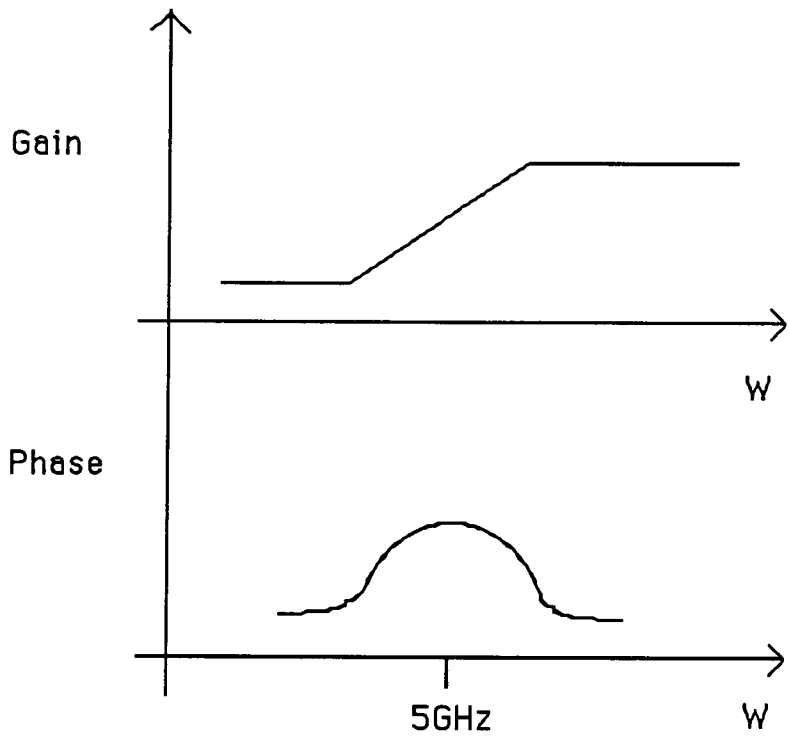


Figure 3.14 Impact of embedded inductor on the phase plot

Replacing the active load with the active inductive load is shown in Figure 3.13. The effective load instead of just being r_d as in the active load case, will be $r_d + jwL\ (1 + gmr_d)$. The derivation is as follows:

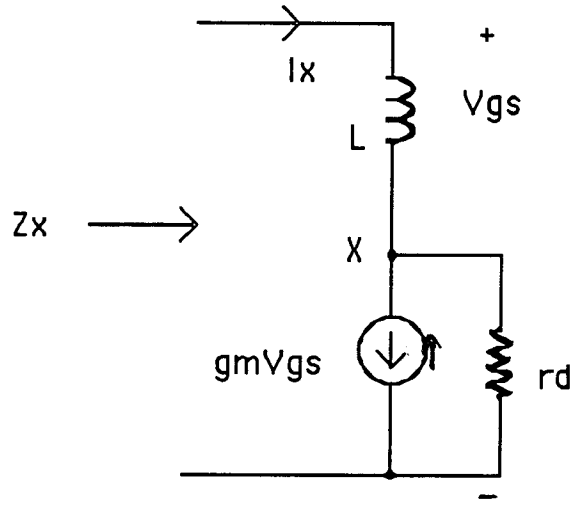


Figure 3.15 AC equivalent circuit of embedded inductor

$V_{gs} = I_x\ jwL$ ----------(1)

KCL at node X,

$$I_x + gm\ V_{gs} - \frac{(V_x - V_{gs})}{r_d} = 0 \quad \text{----------(2)}$$

Solving (1) and (2)

$Z_x = r_d + jwL(1 + gmr_d)$

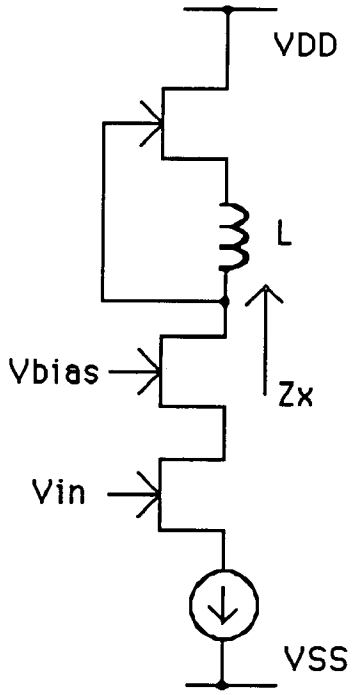


Figure 3.16 Cascode amplifier with inductive compensation

$$A_v = \frac{gmr_d r_d \left[1 + \frac{jwL}{r_d}(1 + gmr_d) \right]}{r_d \left[1 + \frac{jwL}{r_d}(1 + gmr_d) \right]}$$

$$A_v = \frac{gmr_d \left(1 + \frac{jw}{w_a} \right)}{\left(1 + \frac{jw}{w_b} \right)}$$

$$w_a = \frac{L}{r_d}(1 + gmr_d)$$

$$w_b = \frac{L}{2r_d}(1 + gmr_d)$$

$$\text{i.e. } w_b = 2\, w_a$$

$$w_a = \frac{r_d}{L\,(1 + gmr_d)}$$

with L = 6nH

$$w_a = 30 \times 10^9$$

i.e fa = 5 Ghz

Therefore, adding inductor in the circuit can help in the compensation.

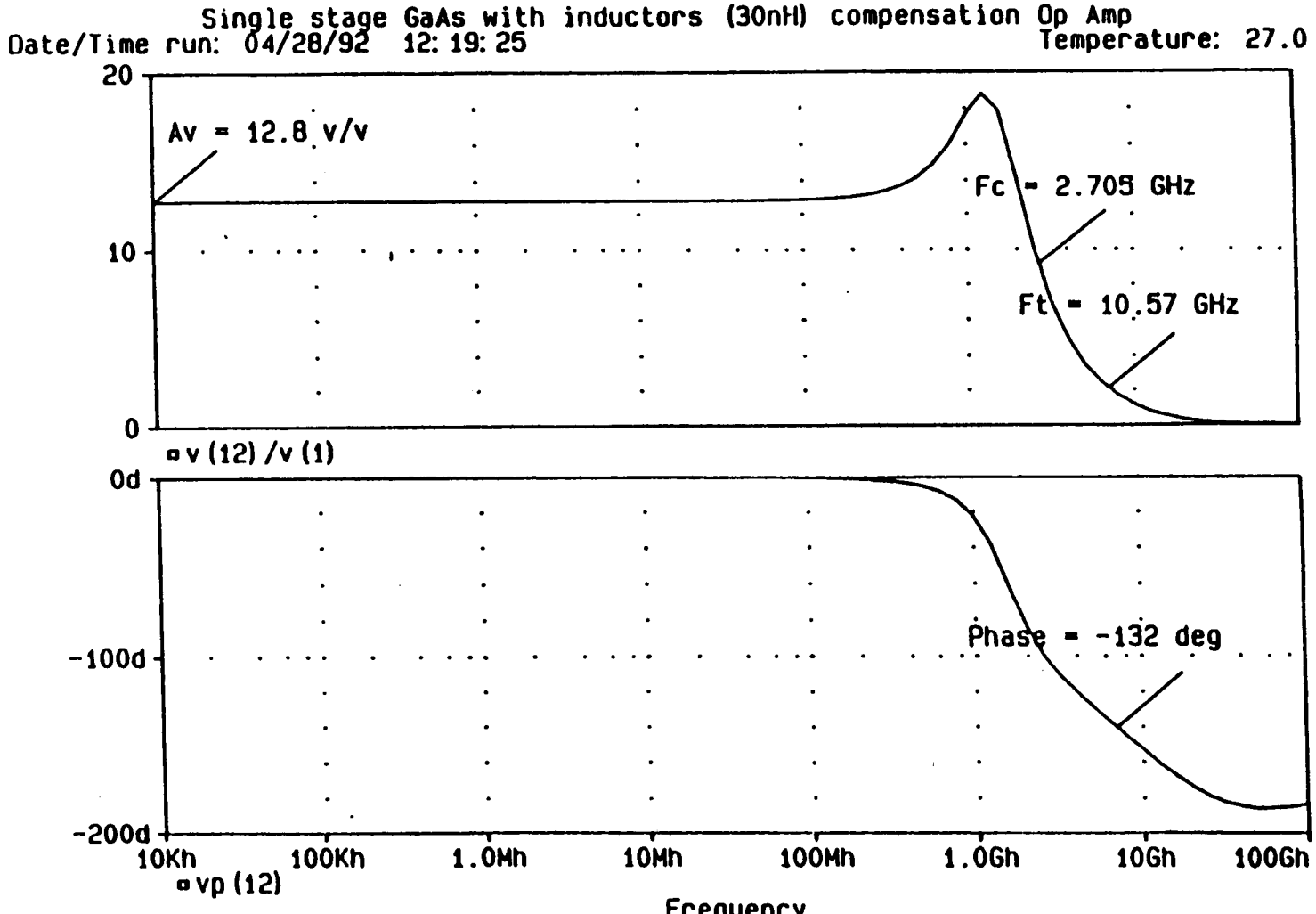


Figure 3.17 Single stage cascode differential amplifier with inductive compensation gain & phase plot

3.4.3 Compensation of composite cascode amplifier

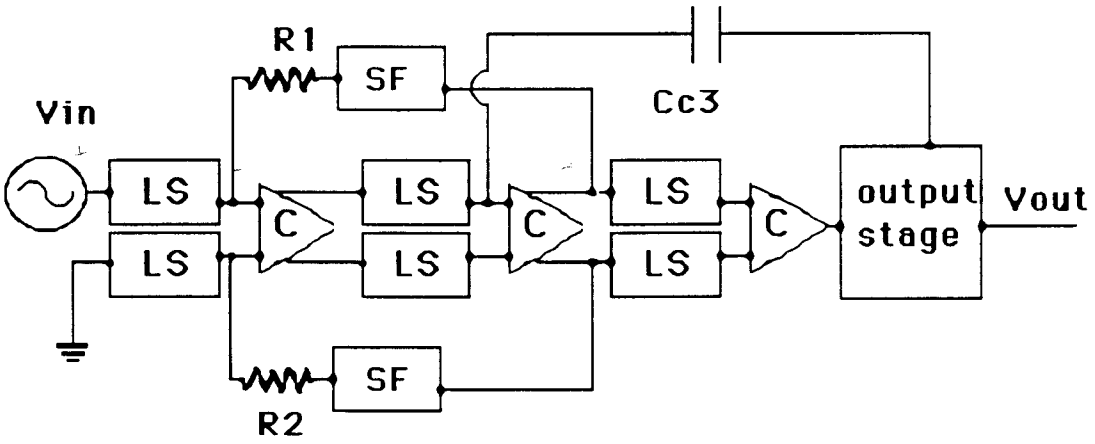


Figure 3.18 Block diagram of compensated composite cascode differential amplifier

R1 (Ω)	R2 (Ω)	Cc3 (fF)	Corner Freq. Fc (Hz)	Unity Gain Freq Ft (Hz)	Phase (degree)	Gain Av (V/v)
-	-	-	526M	9.08G	-537.0	6761
144k	144k	10	119M	8.52G	-124.0	2070
72k	72k	10	201M	8.52G	-124.0	1229
7.5k	7.5k	30	423M	7.71G	-100.0	179
4.5k	4.5k	30	606M	7.71G	-104.0	120
3.5k	3.5k	30	692M	7.71G	-104.0	100
3.5k	3.5k	20	895M	7.84G	-113.0	100
3.5k	3.5k	15	1.04G	7.46G	-108.0	100
3.5k	3.5k	10	1.15G	7.62G	-115.0	100
3.5k	3.5k	5	1.14G	7.78G	-122.0	100
3.5k	3.5k	1	1.03G	7.78G	-128.9	100

Table 3.3 Embedded compensation effect on the composite cascode differential amplifier

The compensation is achieved via R1, R2 and Cc3 as shown in the above Figure 3.18. The technique used with Cc3 is feedforward compensation [18]. On the other hand, the feedback resistor is source followed prior to feedback to prevent any feedforward effects. As can be seen from Table 3.3, the combination R1=3.5k, R2=3.5k and Cc3=10fF has the maximum corner frequency at Fc=1.15GHz, therefore this combination is selected. This is in reality a complex embedded compensation technique.

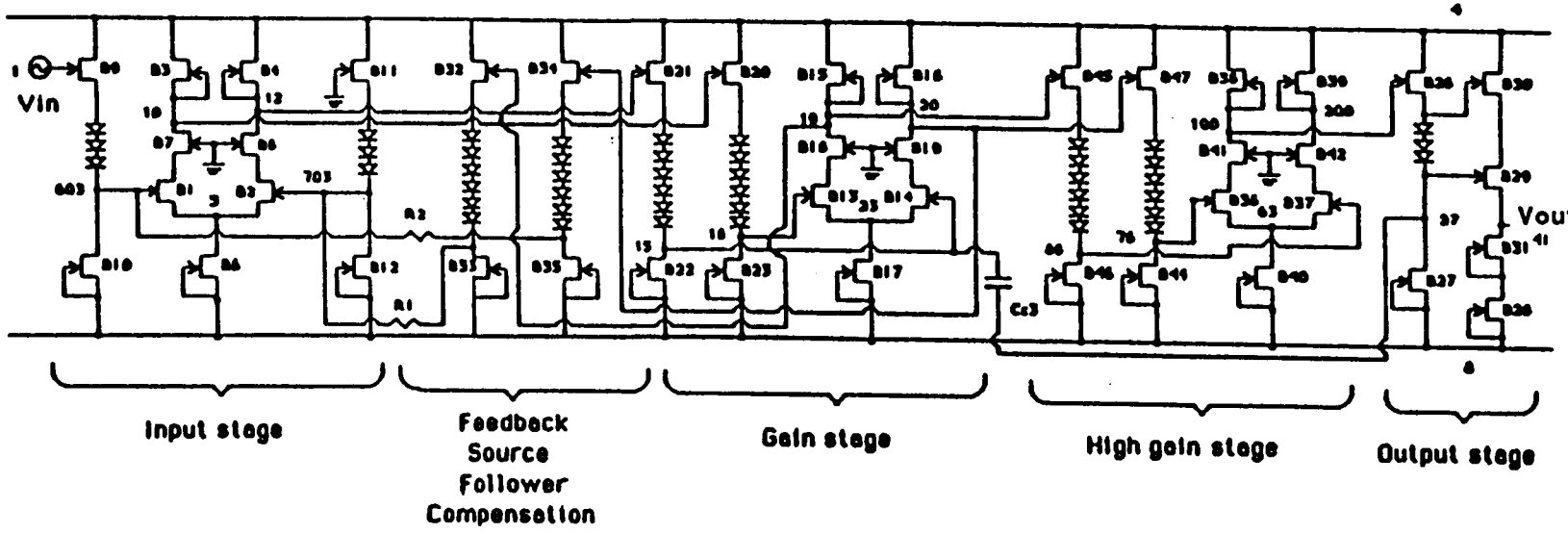


Figure 3.19 Circuit diagram of composite cascode differential amplifier

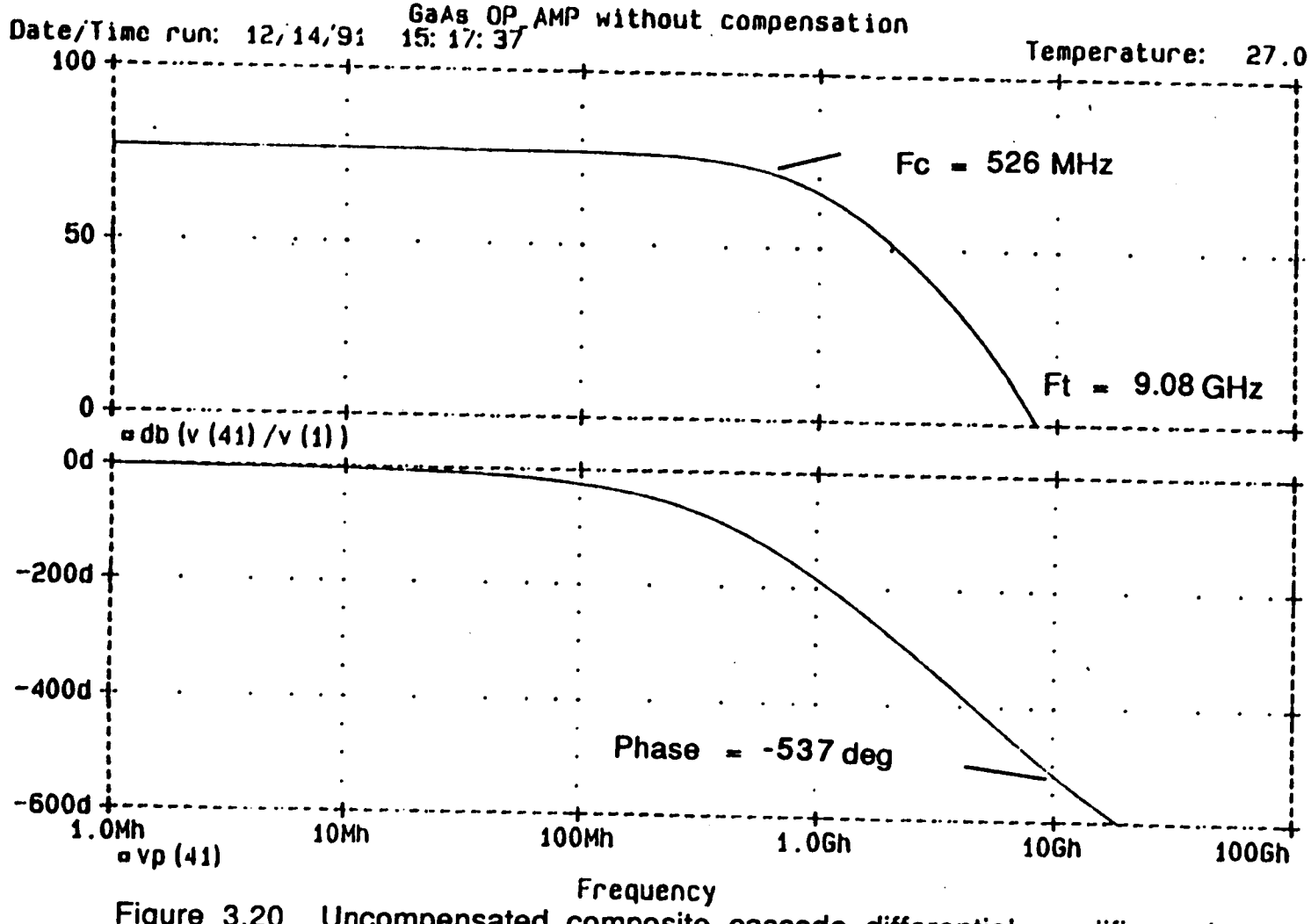


Figure 3.20 Uncompensated composite cascode differential amplifier gain & phase plot

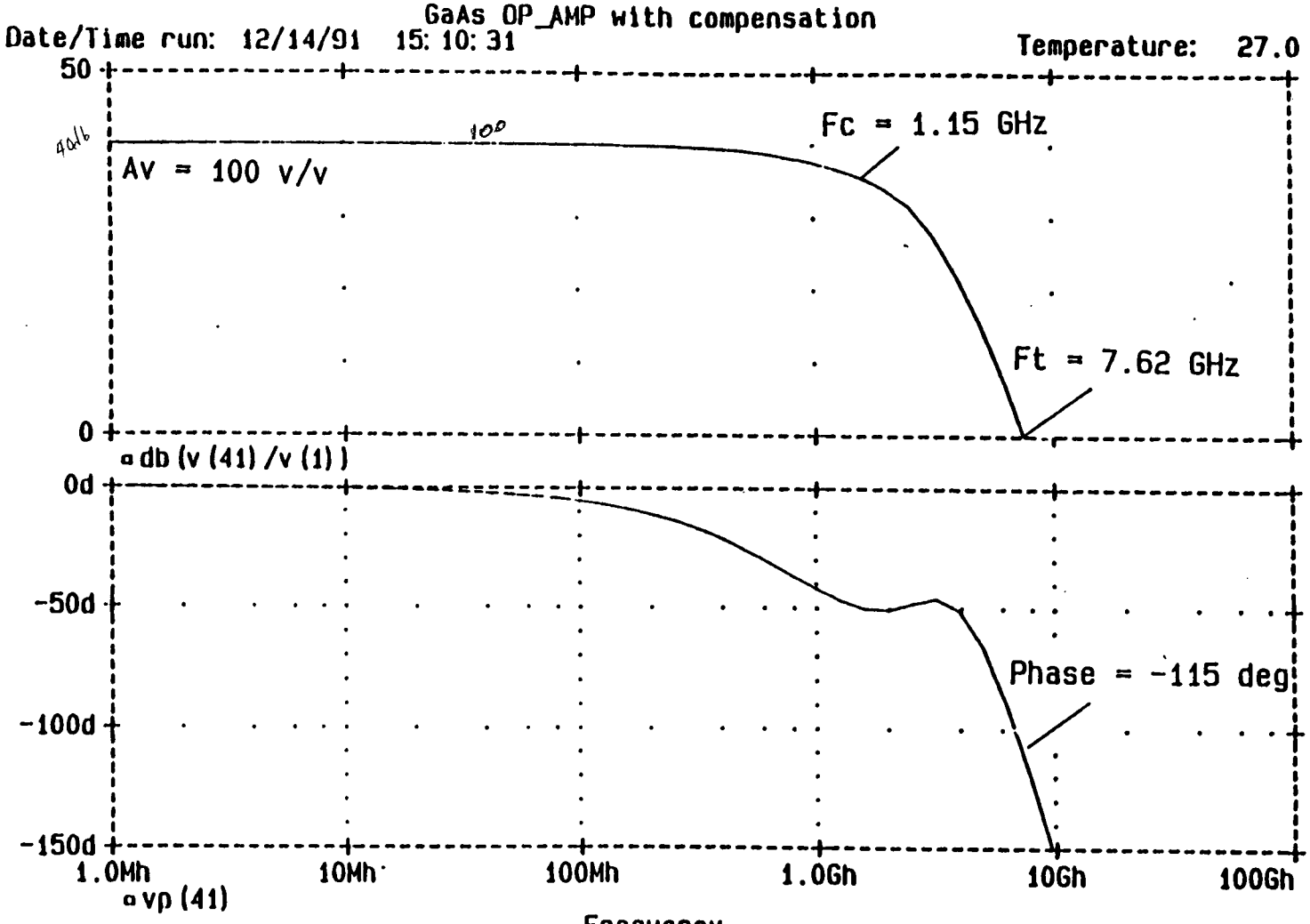


Figure 3.21 Compensated composite cascode differential amplifier gain & phase plot

3.5 Slew Rate Determination

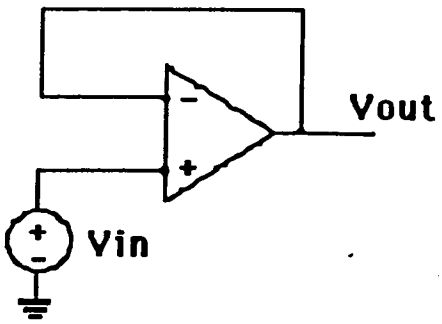


Figure 3.22 Test Circuit for Slew Rate determination

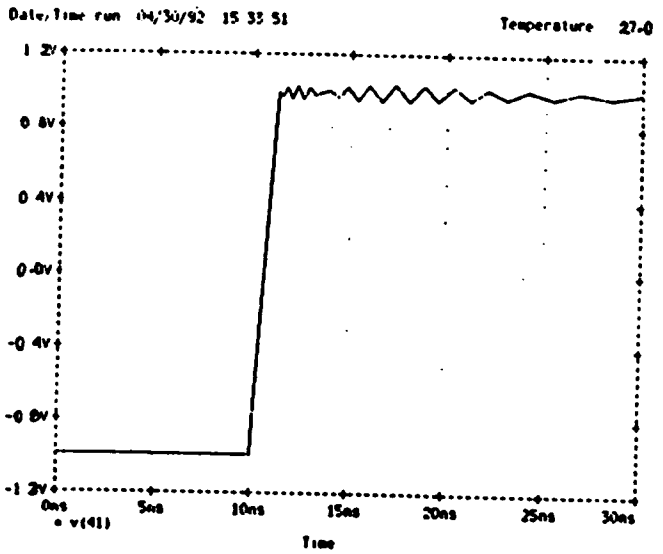


Figure 3.23 Pulse response for +/- 1V step input

To test the large signal performance of the circuit as well as its stability, a step function of +/- 1V is applied at the input. The test circuit shown in Figure 3.22 is configured as unity gain amplifier. The slew rate which is a large signal phenomena can be found this way. The typical value for an MOS operational amplifier is 1 to 20v/μs. However, for our composite cascode differential amplifier the slew rate is 100V/μs for a +/- 1V output swing.

4 Process Variation

4.1 Process variations in the composite cascode differential amplifier

%Δ VTO	VTO	Gain Av (V/V)	%Δ Gain
10	-1.350	110.8	10.8
5	-1.425	105.8	5.80
3	-1.455	103.8	3.80
1	-1.485	101.8	1.80
0	-1.500	100.0	0
-1	-1.515	99.80	0.20
-3	-1.545	97.80	2.20
-5	-1.575	95.80	4.20
-10	-1.650	90.40	9.60

Table 4.1 Composite cascode differential amplifier VTO variation

%Δ lambda	lambda	Gain Av (V/V)	%Δ Gain
10	0.0550	89.9	10.1
5	0.0525	95.1	4.90
3	0.0515	97.3	2.70
1	0.0505	99.6	0.40
0	0.0500	100.0	0
-1	0.0495	102.0	2.00
-3	0.0485	104.6	4.60
-5	0.0475	107.2	7.20
-10	0.0450	114.3	14.3

Table 4.2 Composite cascode differential amplifier Lambda variation

%Δ Beta	Beta	Gain Av (V/v)	%Δ Gain
10	0.0770	104.4	4.40
5	0.0735	102.7	2.70
3	0.0721	102.0	2.00
1	0.0770	101.2	1.20
0	0.0700	100.0	0
-1	0.0693	100.4	0.40
-3	0.0679	99.6	0.40
-5	0.0665	98.7	1.30
-10	0.0630	96.4	3.60

Table 4.3 Composite cascode differential amplifier Beta variation

Normally a 3% change in parameter should not result in a more than 5% change in circuit specification to achieve a reasonable yield of 75%. Table 4.1 shows that a 3% variation in VTO results in a change of 3.8% in gain which is acceptable. Similarly, a +3% change in Lamda results in a 2.7% change in gain. For Beta variations, a +3% change as in Table 4.3 results in a only a 1.2% change in the gain. Thus our Composite Cascode Differential Amplifier is stable under process variations.

4.2 Larson's Circuit

4.2.1 Introduction

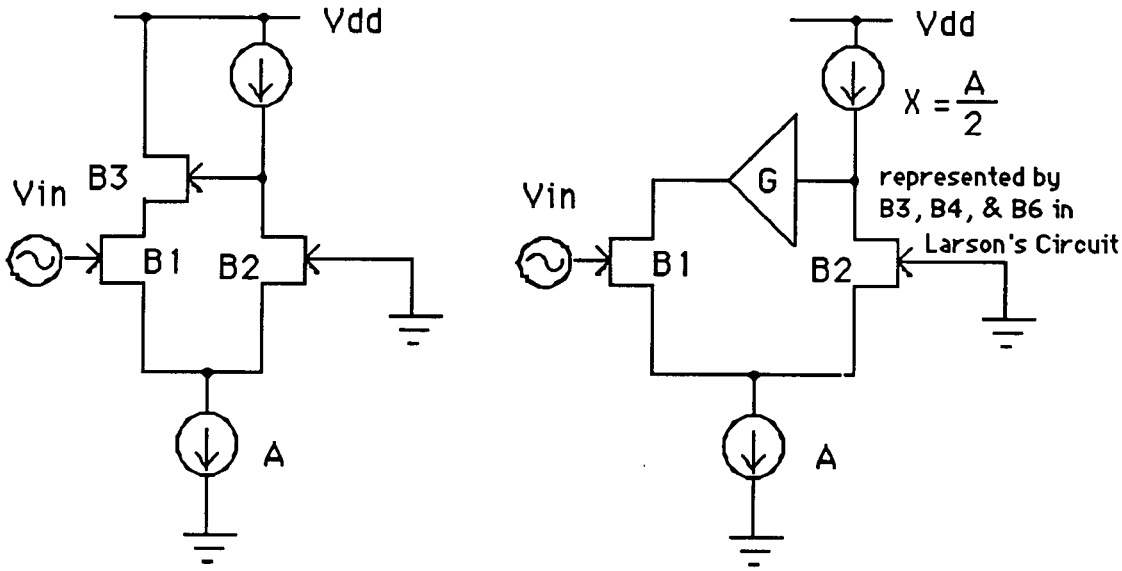


Figure 4.1 Bootstrapped Gain-Enhancement Techniques

Larson's circuit [1] consists of a bootstrapped circuit which is an implementation of Abidi's [19] differential bootstrapped technique as indicated in Figure 4.1.

The high output impedance is obtained by making the positive feedback G close to one.

$$G = \frac{g_{m3} * rds_3}{(1 + g_{m3} * rds_3)}$$

Assuming for identical devices for B1 and B2,

$$Av = \frac{(gm_1 * rds_1)}{(1 - G)}$$

4.2.2 Larson's Circuit Diagram

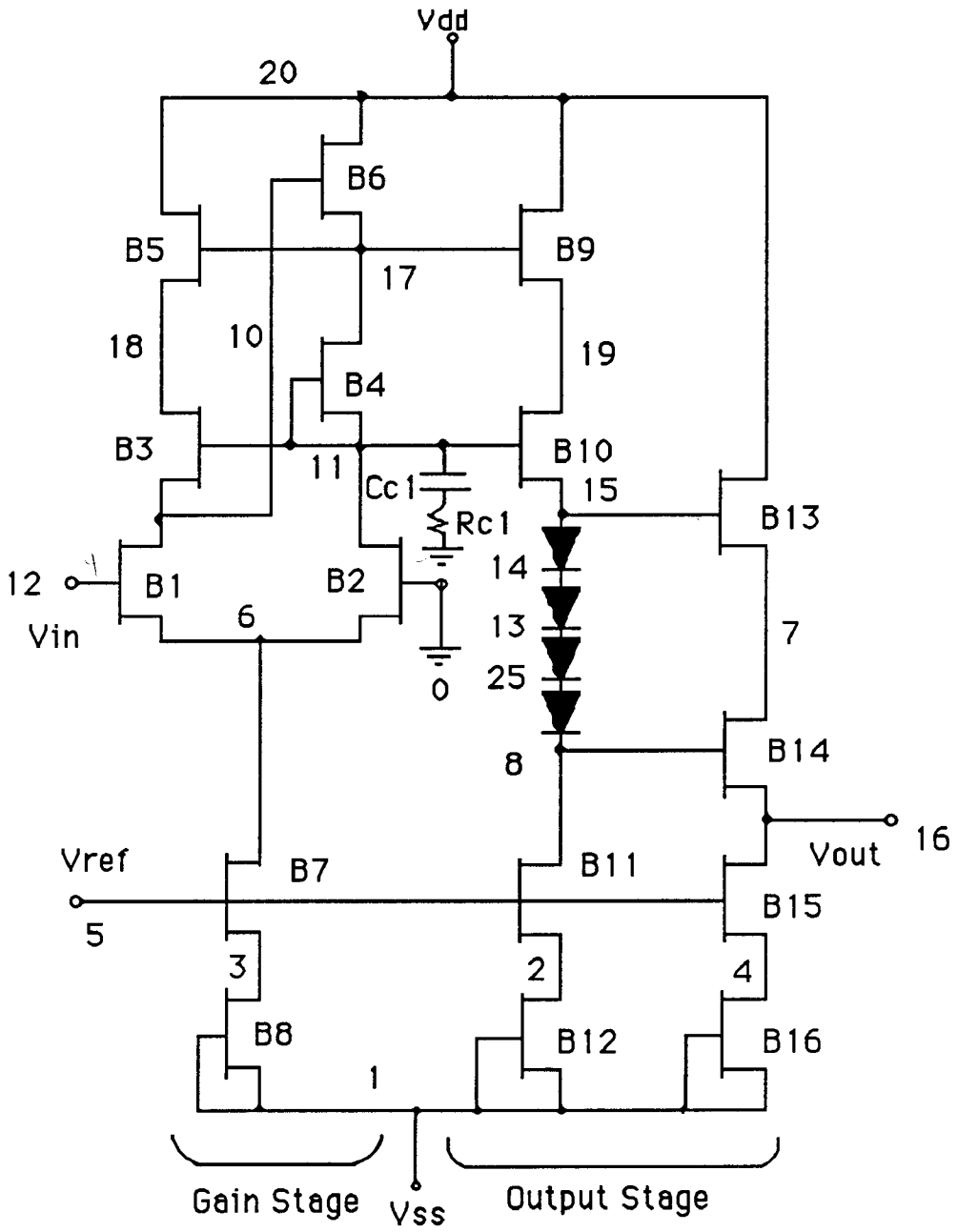


Figure 4.2 Larson's GaAs operational amplifier

Larson extended on Abidi's idea by implementing the current source X by using B3, B4 and B6 as in Figure 4.2. The source follower action of B3 and B6 ensure that B4 is always saturated. Sizing B3 and B6 to be 4 times that of B4 helps to ensure that the first stage works over a large range of bias conditions. This configuration will also result in a high output impedance at the source of B4.

$$Av = \frac{(g_{m3} * rds_3 * g_{m6} * rds_6 * rds_4 * g_{m1})}{2(g_{m6} * rds_6 + g_{m3} * rds_3)}$$

For the first stage the gain at output node (11) is = 114. The overall gain of the complete amplifier is 109. All gain that is required is provided by the first stage with some degradation after passing through the level shifter and output stage.

The source follower action of B9 and B10 help to transfer voltage at node 11 and 17 with minimal drop at node 19 and 15 respectively. The MESFET connected diodes helps to achieve a zero offset voltage.

By reducing the width of any MESFET connected diodes, which increases the effective resistance, a higher Vd can be obtained. Therefore, an accurate zero output offset voltage can be readily obtained by adjusting the width of the device.

The output offset voltage of this stage is = 0.477V. The output resistance is 50.4Ω to match the specified output load 50Ω. This

ensures as little reflection back into the output node as possible. The 50.4Ω output resistance is obtained by varying the width of B13, B14, B15, and B16.

For stability, the circuit needs to be compensated by a pole zero cancellation technique via Cc1 and Rc1

Vref (Volts)	Gain (Av)	Wc (MHz)	Wt (GHz)	Phase (Degree)
-2.0	14.9	323.0	3.8	-115.7
-3.0	57.6	85.0	3.6	-111.0
-3.1	79.0	60.0	3.8	-111.0
-3.2	108.0	42.0	3.8	-110.0
-3.3	108.0	42.0	3.8	-108.0
-3.4	76.0	55.1	3.8	-107.0
-3.5	51.0	80.0	3.6	-105.0
-4.0	9.2	85.0	2.5	-94.0

Table 4.4 Variation of overall gain with different Vref biasing

The above table show circuit parameter variations with different values of Vref. Depending on the requirement of the user, there is a trade off of lower band width for higher gain.

The overall voltage gain can be increased to 248.9 by choosing a device width of 4000μm for B1, B2 and B5. These unrealistic values will substantially increase the area required. This will also defeat the purpose of the bootstrapped circuit which uses substantially more devices compared to the traditional circuit implementation.

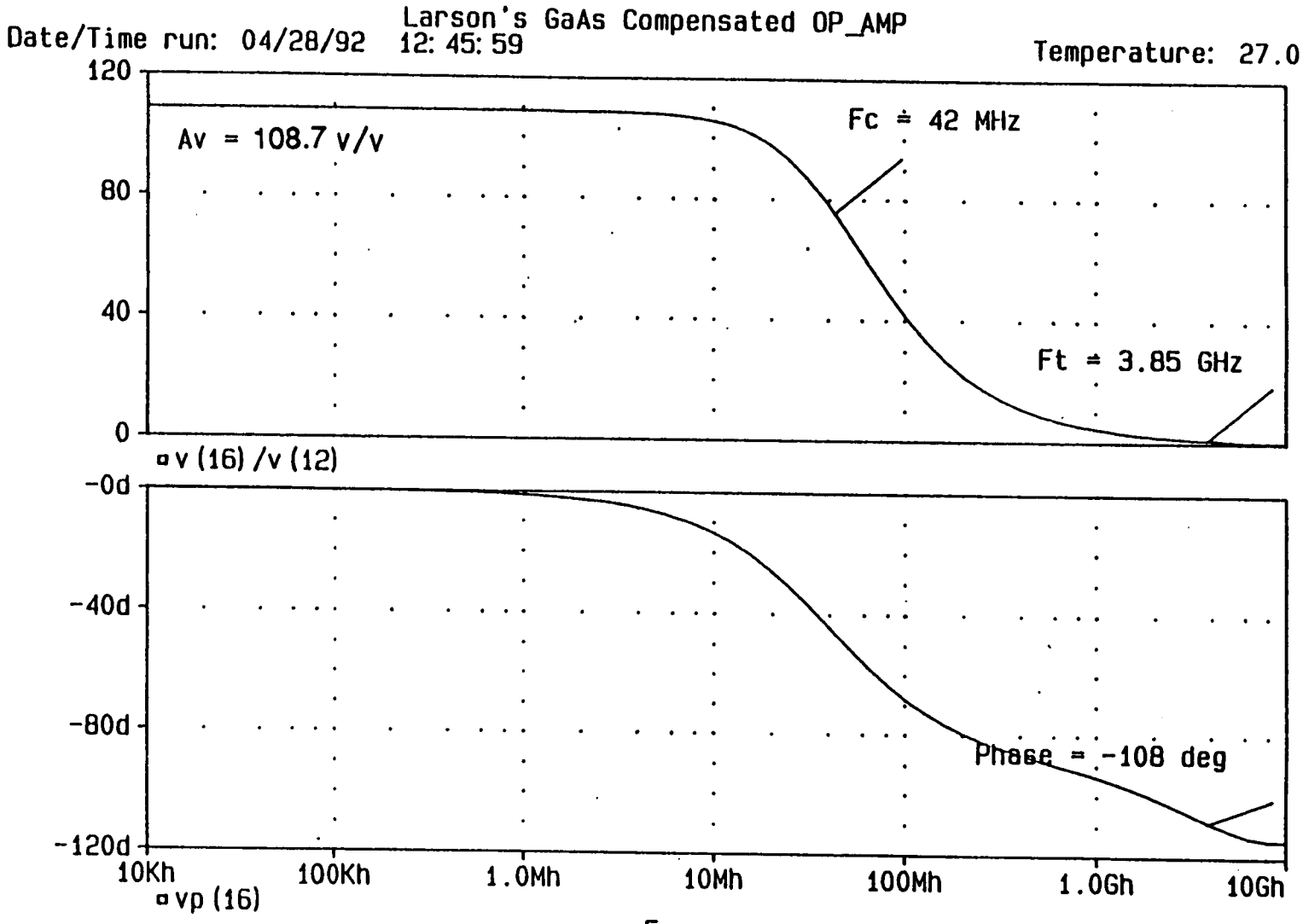


Figure 4.3 Larson's circuit gain & phase plot

4.2.3 Process variations in the Larson's Circuit

%Δ in VTO	VTO (V)	Gain Av(v/v)	%Δ in Gain
10	-1.350	72.8	33.0
5	-1.425	124.0	14.1
3	-1.455	132.5	21.9
1	-1.485	119.2	9.66
0	-1.500	108.7	0
- 1	-1.515	98.1	9.75
- 3	-1.545	80.1	26.3
- 5	-1.575	66.5	38.8
- 10	-1.650	45.0	58.6

Table 4.5 Larson's amplifier VTO variation

%Δ in Lambda	lambda	Gain Av (v/v)	%Δ in gain
10	0.0550	103.3	4.97
5	0.0525	105.9	2.58
3	0.0515	107.0	1.56
1	0.0505	108.1	0.55
0	0.0500	108.7	0
-1	0.0495	109.2	0.45
-3	0.0485	110.4	1.56
-5	0.0475	111.6	2.68
-10	0.0450	114.7	5.52

Table 4.6 Larson's amplifier Lambda variation

%Δ in Beta	Beta	Gain Av (v/v)	%Δ in gain
10	0.0770	105.5	2.94
5	0.0735	106.8	1.75
3	0.0721	107.8	0.83
1	0.0770	108.3	0.37
0	0.0700	108.7	0
-1	0.0693	109.1	0.37
-3	0.0679	109.8	1.01
-5	0.0665	110.6	1.74
-10	0.0630	112.6	3.58

Table 4.7 Larson's amplifier Beta variation

As mentioned in section 4.1, for the TriQuint 1 processes, a +/-3% change in process parameters should result in no more than 5% change in gain in order to achieve a reasonable yield. Table 4.5 shows clearly that a VTO change of 3% result in a corresponding change of 21.9% in gain. On the other hand, Table 4.6 and Table 4.7 show that the circuit is more tolerable to Lamda and Beta variations.

Furthermore, the circuit is extremely sensitive to variation in the device width of B3, B4 and B6. To optimize the voltage gain the widths of B6 and B3 have to be 4 times that of B4, a rule which has to be followed. In addition, to get maximum voltage gain, the Vref has to be biased fairly accurately. As shown for the 1μm technology results, the Vref has to be between -3.2 to 3.3V to obtain a gain of

109. Any variation of Vref will substantially degrade the voltage gain. For instance, a circuit with Vref=-3.5 has a voltage gain cut by half to 51.

4.3 Toumazou's Circuit

4.3.1 Introduction

The following is a GaAs operational amplifier proposed by Toumazou [20] [21] [22].

4.3.2 Toumazou's Circuit Diagram

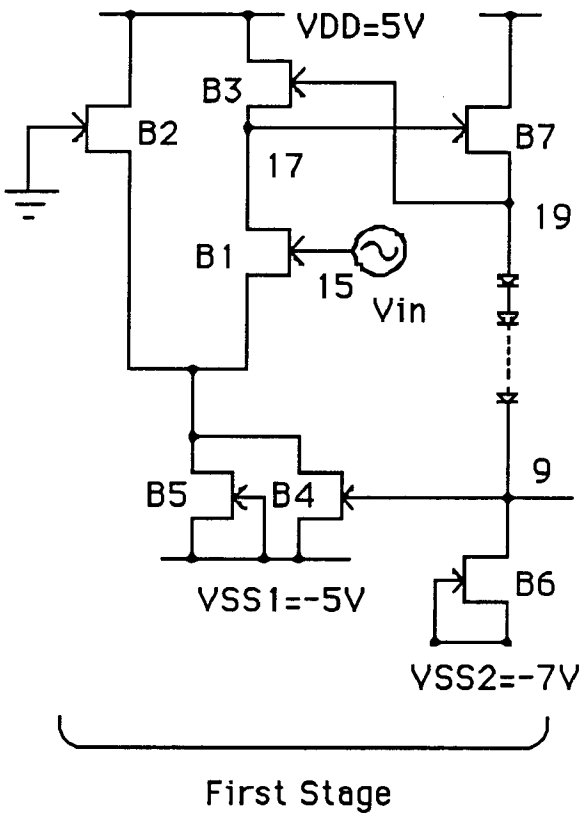


Figure 4.4 First Stage or Differential to Single-ended converter of Toumazou's Composite Operational Amplifier

The first stage is a differential to a single-ended converter. B3 and B7 represent the a current mirror with their gates and sources cross coupled. The gain of the first stage is constrained by

the biasing requirement of the second or gain stage. As will be shown later, optimum biasing occurs when the output node 9, as shown in the Figure 4.4 is set as closed to DC -5V as possible. By varying the width of the MESFET connected diodes, a level shifted DC bias point of -5.0026V is obtained for the critical node 9. With this constrained the gain attainable from the first stage is relatively low at approximately 4.86.

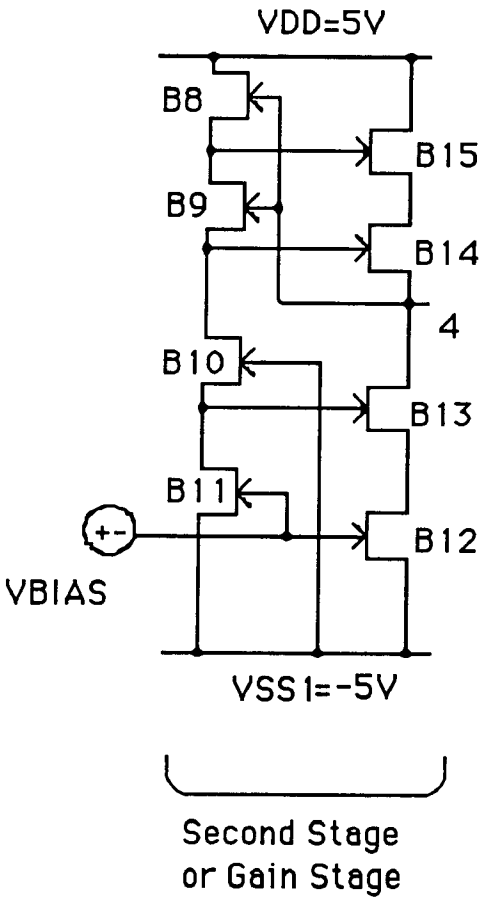


Figure 4.5 Second Stage or Double Cascode Current Mirror and Push-pull Amplifier of Toumazou's Composite Operational Amplifier

VBAIS (V)	Gain Av(v/v)
-4.00	0.8
-4.90	3.2
-4.95	7.7
-4.99	88.9
-5.00	355.0
-5.01	88.0
-5.10	4.0

Table 4.8 The effect of biasing on the critical node 9.

With proper biasing, the second stage can provide a gain of 355. The second stage is configured as a double cascode current mirror and push-pull amplifier. It is extremely sensitive to VBIAS changes as indicated in Table 4.11.

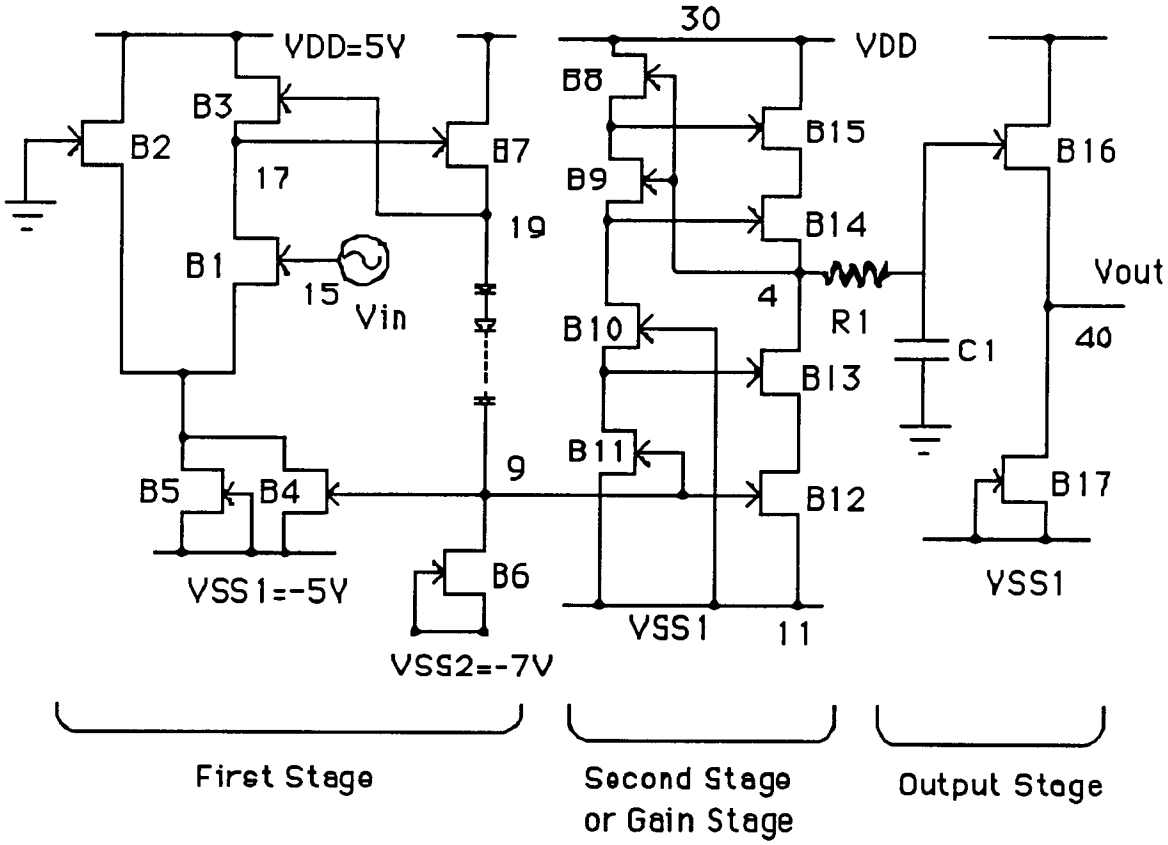


Figure 4.6 Complete Toumazou's Composite Operational Amplifier with Compensation

Thus a composite amplifier consisting of the first stage and the second stage can be obtained as in Figure 4.5. The output stage is a Class A design with the width of B16 and B17 set at 100μm so as the output impedance at node 40 is set as closed to 50Ω as possible. The large areas of B16 and B17 account for this reduced impedance. The circuit is compensated using the pole zero cancellation compensation technique as indicated by R1 and C1.

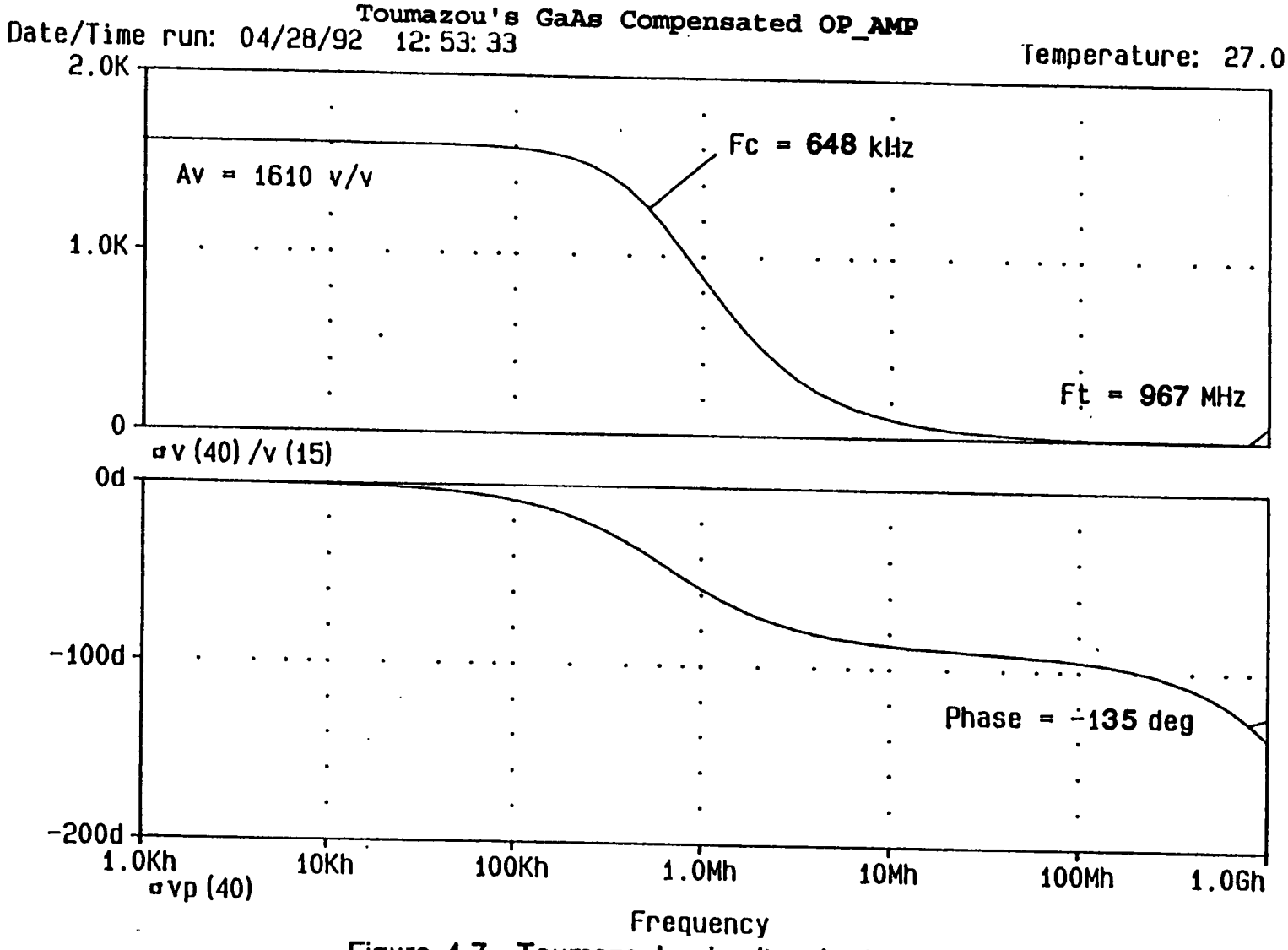


Figure 4.7 Toumazou's circuit gain & phase plot

After compensation, an open loop gain of 1610, corner frequency of 648.6KHz and a unity gain frequency of 967MHz are obtained for a compensated phase margin of 43.5 degree.

The following tables represent the effect of process variations. The drastic changes in the value of the gain indicate that the circuit is sensitive to process variations.

4.3.3 Process variations in the Toumazou's Circuit

%Δ in VTO	VTO (V)	Gain Av (v/v)	%Δ in Gain
10	-1.350	6.7	99.6
5	-1.425	20.0	98.8
3	-1.455	43.0	97.3
1	-1.485	246	84.7
0	-1.500	1610	0
- 1	-1.515	237	85.3
- 3	-1.545	52.7	96.7
- 5	-1.575	28.9	98.2
- 10	-1.650	13.7	99.1

Table 4.9 Toumazou's amplifier VTO variation

%Δ Lambda	Lambda	Gain Av (v/v)	%Δ in Gain
10	0.0550	932.0	42.1
5	0.0525	1484.0	7.83
3	0.0515	1546.0	3.98
1	0.0505	1590.0	1.24
0	0.0500	1610.0	0
-1	0.0495	1660.2	1.12
-3	0.0485	1665	3.04
-5	0.0475	1671.0	3.70
-10	0.0450	852.0	41.1

Table 4.10 Toumazou's amplifier Lambda variation

%Δ Beta	Beta	Gain Av(v/v)	%Δ in Gain
10	0.0770	46.2	97.1
5	0.0735	105.7	93.4
3	0.0721	214.8	86.7
1	0.0770	1437.0	10.7
0	0.0700	1610.0	0
-1	0.0693	1478.0	8.20
-3	0.0679	200.0	87.6
-5	0.0665	86.2	94.6
-10	0.0630	28.9	98.2

Table 4.11 Toumazou's amplifier Beta variation

For a reasonable yield of above 75%, a +/-3% change in a parameter should not result in more than 5% change in circuit specifications. Table 4.9 and Table 4.10 show that the Toumazou's circuit could not withstand a 3% change in VTO and Beta.

4.4 Circuit process variations conclusion

For a Lamda parameter variation all three circuits meet the 3% process variation as shown in the Tables from section 4.1 through 4.3, Toumazou's circuit fails to meet the yield requirement for Beta and VTO variations. Larson's circuit is better when compared to Toumazou's design, however, Larson's circuit fails the VTO process variation test.

Our composite differential amplifier is more resistant to process variations, thus our principle objective is accomplished. It is superior to Larson's circuit because it does not require an accurate biasing at Vref. This accurate biasing requirement resulted in Larson's circuit not being commercially viable with the current depletion MESFET processes. In the same manner, Toumazou's circuit contains a critical node 9 which need to be accurately biased to achieve any gain. Given the maturity of the current commercially available technology, our circuit is predicted to be to have a higher yield rate.

5. Summary

GaAs MESFET technology has not reached the state of maturity when compared to Silicon MOSFET's or bipolars to be a viable threat yet. As the technology improves, better process control will bring higher yields which ultimately will mean a higher level of circuit integration. The higher speed advantage of GaAs MESFET's over silicon cannot be ignored and would be the main driving force behind MESFET device modelling and fabrication technology improvements.

The simple Curtice model is selected in view of the fact that the circuit we have designed is not targeted for use in large-signal microwave applications and that our process parameters which have been chosen from TriQuint Semiconductor have a reasonable pinch off voltage of -1.5V. The Curtice or PSpice level 1 circuit model works well if the transistors operate near Idss. However if the devices operate at small fraction of I_{dss} and /or low V_{ds}, the drain-to-source resistance r_{ds} does not increase as much as Pspice predicts. The Curtice model is not an accurate predictor for circuit behavior over a wide range of I_{ds} and V_{gs}. These limitations of the modelling have been observed and our circuit is designed so as not to violate these constraints.

Our composite cascode differential amplifier has a high bandwidth of 1.15 GHz. It has been simulated using a PSpice level 1 circuit model with TriQuint Semiconductor 1μm depletion mode

parameters. Different kinds of compensation techniques have been investigated and the complex embedded compensation technique proved to be most suitable for our particular design.

Our circuit is also found to be more stable with respect to process variations when compared to Toumazou's and Larson's circuits. As such, it is anticipated that the yield of our design is higher, thus making it commercially viable with the present technology.

As the demand for satellite , optical and other mass communication systems increases, the need for high speed circuits operating into the tens of gigahertz will be higher. Therefore, an interesting follow-on to this work might be to simulate the circuit using reduced gate lengths of 0.5μm so as to obtain higher speed.

In addition, to make the simulation more realistic, the operational amplifier should be resimulated with wiring inductance at all its inputs and output. Dominant parasitic capacitances and inductors from the layout should be included in the simulation. Another area of future work may be to resimulate circuit to investigate the power supply tolerance and also the noise.

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7. Appendices

Appendix 1. PSpice simulation for the composite cascode differential amplifier with Class A output stage

```
VDD 4 0 DC 5
VSS 8 0 DC -5
VIN1 1 0 AC 1m
*
** First stage cascode differential amplifier
B1     2    603 3    G1 0.02
B2     5    703 3    G1 0.02
B3     4    10  10   G1 0.02
B4     4    12  12   G1 0.02
B6     3    8   8    G1 0.04
B7     10   0   2    G1 0.02
B8     12   0   5    G1 0.02
*
*
** First stage input level shifter to -2.5V
B9     4    1   600 G1 0.02
B10    603  8   8   G1 0.02
BD1    600  600 601 G1 0.013
BD2    601  601 602 G1 0.013
BD3    602  602 603 G1 0.013
*
B11    4    0   700 G1 0.02
B12    703  8   8   G1 0.02
BD4    700  700 701 G1 0.013
BD5    701  701 702 G1 0.013
BD6    702  702 703 G1 0.013
*
** Second stage cascode differential amplifier
B13    21   18  23  G1 0.02
B14    22   15  23  G1 0.02
B15    4    19  19  G1 0.02
B16    4    20  20  G1 0.02
B17    23   8   8   G1 0.04
B18    19   0   21  G1 0.02
B19    20   0   22  G1 0.02
*
** Second stage input level shifter to -2.5V
B21    4    12  13  G1 0.02
BD7    13   13  14  G1 0.013
BD8    14   14  140 G1 0.013
BD9    140  140 141 G1 0.013
BD10   141  141 142 G1 0.013
BD11   142  142 143 G1 0.013
BD12   143  143 15  G1 0.013
B22    15   8   8   G1 0.02
*
```

```
B20    4    10   16   G1 0.02
BD13   16   16   17   G1 0.013
BD14   17   17   170  G1 0.013
BD15   170  170  171  G1 0.013
BD16   171  171  172  G1 0.013
BD17   172  172  173  G1 0.013
BD18   173  173  18   G1 0.013
B23    18   8    8    G1 0.02

* Feedback #1 source follower & level shifter to -2.5V
B32    4    19   200  G1 0.02
BD19   200  200  201  G1 0.013
BD20   201  201  202  G1 0.013
BD21   202  202  203  G1 0.013
BD22   203  203  204  G1 0.013
BD23   204  204  205  G1 0.013
BD24   205  205  206  G1 0.013
B33    206  8    8    G1 0.02
*
* Feedback #2 source follower & level shifter to -2.5V
B34    4    20   300  G1 0.02
BD28   300  300  301  G1 0.013
BD29   301  301  302  G1 0.013
BD30   302  302  303  G1 0.013
BD31   303  303  304  G1 0.013
BD32   304  304  305  G1 0.013
BD33   305  305  306  G1 0.013
B35    306  8    8    G1 0.02
*
** Third stage cascode differential amplifier
B36    61   75   63    G1 0.02
B37    62   88   63    G1 0.02
B38    4    190  190   G1 0.02
B39    4    200   200  G1 0.02
B40    63   8    8     G1 0.04
B41    190  0    61    G1 0.02
B42    200  0    62    G1 0.02
*
** Third stage input level shifter to -2.5V
B43    4    20   73    G1 0.02
BD34   73   73   74    G1 0.013
BD35   74   74   740   G1 0.013
BD36   740  740  741   G1 0.013
BD37   741  741  742   G1 0.013
BD38   742  742  743   G1 0.013
BD39   743  743  75    G1 0.013
B44    75   8    8     G1 0.02
*
B45    4    19   86    G1 0.02
BD40   86   86   87    G1 0.013
BD41   87   87   870   G1 0.013
BD42   870  870  871   G1 0.013
BD43   871  871  872   G1 0.013
BD44   872  872  873   G1 0.013
BD45   873  873  88    G1 0.013
B46    88   8    8     G1 0.02
*
*
** OUTPUT STAGE
B26    4    190  24   G1 0.02
```

```
B27   27  8    8   G1 0.02
BD25  24  24   25  G1 0.015
BD26  25  25   26  G1 0.015
BD27  26  26   27  G1 0.015
*
B28   42  8    8   G1 0.114
B29   40  27   41  G1 0.114
B30   4   24   40  G1 0.114
B31   41  42   42  G1 0.114
*
** Compensation
R1    206 703 3.5K
R2    306 603 3.5K
Cc3    15  27  10f
*
** ANALYSIS
*
.MODEL G1 GASFET(level=1 VTO=-1.5  BETA=0.07 LAMBDA=0.05 RD=1 RS=1
+                VBI=0.8 CGS=0.5E-12 CGD=0.5E-12 IS=1E-14 FC=0.5)
.TF V(41) VIN1
.OP
.AC DEC 10 1MEG 100G
.PROBE
.END
```

******* 12/14/91 ******* PSpice 4.03 - January, 1990 ******* 15:15:04

GaAs OP_AMP with compensation

**** GaAs MESFET MODEL PARAMETERS

****

	G1
LEVEL	1
VTO	-1.5
VBI	.8
ALPHA	2
B	.3
BETA	.07
LAMBDA	.05
RD	1
RS	1
CGD	500.000000E-15
CGS	500.000000E-15

******* 12/14/91 ******* PSpice 4.03 - January, 1990 ******* 15:15:04 *******

GaAs OP_AMP with compensation

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	-424.3E-06	(3)	-2.4931	(4)	5.0000
(5)	-414.9E-06	(8)	-5.0000	(10)	2.4930	(12)	2.4932
(13)	2.4964	(14)	1.6473	(15)	-2.5978	(16)	2.4962
(17)	1.6472	(18)	-2.5979	(19)	2.5938	(20)	2.5900
(21)	.0057	(22)	.0055	(23)	-2.5919	(24)	2.4886
(25)	1.6762	(26)	.8638	(27)	.0514	(40)	2.4882
(41)	.0487	(42)	-2.4756	(61)	.0039	(62)	.0018
(63)	-2.5167	(73)	2.5879	(74)	1.7367	(75)	-2.5193
(86)	2.5914	(87)	1.7401	(88)	-2.5163	(140)	.7983
(141)	-.0507	(142)	-.8997	(143)	-1.7487	(170)	.7982
(171)	-.0508	(172)	-.8998	(173)	-1.7489	(190)	2.5636
(200)	2.5891	(201)	1.7390	(202)	.8890	(203)	.0389
(204)	-.8112	(205)	-1.6612	(206)	-2.5113	(300)	2.5891
(301)	1.7391	(302)	.8890	(303)	.0389	(304)	-.8111
(305)	-1.6612	(306)	-2.5112	(600)	.0672	(601)	-.7861
(602)	-1.6394	(603)	-2.4926	(700)	.0672	(701)	-.7861
(702)	-1.6394	(703)	-2.4926	(740)	.8855	(741)	.0343
(742)	-.8169	(743)	-1.6681	(870)	.8888	(871)	.0376
(872)	-.8137	(873)	-1.6650				

VOLTAGE SOURCE CURRENTS
NAME CURRENT

VDD	-5.948E-02
VSS	5.948E-02
VIN1	5.068E-12

TOTAL POWER DISSIPATION 5.95E-01 WATTS

******* 12/14/91 ******* PSpice 4.03 - January, 1990 ******* 15:15:04 **

GaAs OP_AMP with compensation

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** GASFETS

NAME	B1	B2	B3	B4	B6
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.86E-03	2.86E-03	5.73E-03
VGS	4.48E-04	4.43E-04	0.00E+00	0.00E+00	0.00E+00
VDS	2.49E+00	2.49E+00	2.51E+00	2.51E+00	2.51E+00
GM	4.22E-03	4.22E-03	4.22E-03	4.22E-03	8.44E-03
GDS	1.32E-04	1.32E-04	1.32E-04	1.32E-04	2.64E-04
CGS	9.21E-15	9.21E-15	9.21E-15	9.21E-15	1.84E-14
CGD	5.04E-15	5.04E-15	5.03E-15	5.03E-15	1.01E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B7	B8	B9	B10	BD1
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.87E-03	2.86E-03	2.86E-03
VGS	4.24E-04	4.15E-04	-6.72E-02	0.00E+00	8.53E-01
VDS	2.49E+00	2.49E+00	4.93E+00	2.51E+00	8.53E-01
GM	4.22E-03	4.22E-03	4.45E-03	4.22E-03	2.68E-03
GDS	1.32E-04	1.32E-04	1.16E-04	1.32E-04	4.71E-03
CGS	9.21E-15	9.21E-15	8.90E-15	9.21E-15	1.19E-14
CGD	5.04E-15	5.04E-15	3.76E-15	5.03E-15	7.64E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD2	BD3	B11	B12	BD4
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.87E-03	2.86E-03	2.86E-03
VGS	8.53E-01	8.53E-01	-6.72E-02	0.00E+00	8.53E-01
VDS	8.53E-01	8.53E-01	4.93E+00	2.51E+00	8.53E-01
GM	2.68E-03	2.68E-03	4.45E-03	4.22E-03	2.68E-03
GDS	4.71E-03	4.71E-03	1.16E-04	1.32E-04	4.71E-03
CGS	1.19E-14	1.19E-14	8.90E-15	9.21E-15	1.19E-14
CGD	7.64E-15	7.64E-15	3.76E-15	5.03E-15	7.64E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD5	BD6	B13	B14	B15
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.53E-01	8.53E-01	-5.98E-03	-5.86E-03	0.00E+00
VDS	8.53E-01	8.53E-01	2.60E+00	2.60E+00	2.41E+00
GM	2.68E-03	2.68E-03	4.22E-03	4.22E-03	4.20E-03
GDS	4.71E-03	4.71E-03	1.30E-04	1.30E-04	1.34E-04

CGS	1.19E-14	1.19E-14	9.18E-15	9.18E-15	9.21E-15
CGD	7.64E-15	7.64E-15	4.95E-15	4.95E-15	5.11E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	B16	B17	B18	B19	B21
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	5.70E-03	2.85E-03	2.85E-03	2.85E-03
VGS	0.00E+00	0.00E+00	-5.69E-03	-5.46E-03	-3.20E-03
VDS	2.41E+00	2.41E+00	2.59E+00	2.58E+00	2.50E+00
GM	4.20E-03	8.40E-03	4.22E-03	4.22E-03	4.21E-03
GDS	1.34E-04	2.67E-04	1.30E-04	1.30E-04	1.32E-04
CGS	9.21E-15	1.84E-14	9.18E-15	9.19E-15	9.20E-15
CGD	5.11E-15	1.02E-14	4.96E-15	4.96E-15	5.03E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	BD7	BD8	BD9	BD10	BD11
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.49E-01	8.49E-01	8.49E-01	8.49E-01	8.49E-01
VDS	8.49E-01	8.49E-01	8.49E-01	8.49E-01	8.49E-01
GM	2.67E-03	2.67E-03	2.67E-03	2.67E-03	2.67E-03
GDS	4.72E-03	4.72E-03	4.72E-03	4.72E-03	4.72E-03
CGS	1.18E-14	1.18E-14	1.18E-14	1.18E-14	1.18E-14
CGD	7.63E-15	7.63E-15	7.63E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	BD12	B22	B20	BD13	BD14
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.49E-01	0.00E+00	-3.20E-03	8.49E-01	8.49E-01
VDS	8.49E-01	2.40E+00	2.50E+00	8.49E-01	8.49E-01
GM	2.67E-03	4.20E-03	4.21E-03	2.67E-03	2.67E-03
GDS	4.72E-03	1.34E-04	1.32E-04	4.72E-03	4.72E-03
CGS	1.18E-14	9.21E-15	9.20E-15	1.18E-14	1.18E-14
CGD	7.63E-15	5.11E-15	5.03E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	BD15	BD16	BD17	BD18	B23
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.49E-01	8.49E-01	8.49E-01	8.49E-01	0.00E+00
VDS	8.49E-01	8.49E-01	8.49E-01	8.49E-01	2.40E+00
GM	2.67E-03	2.67E-03	2.67E-03	2.67E-03	4.20E-03
GDS	4.72E-03	4.72E-03	4.72E-03	4.72E-03	1.34E-04
CGS	1.18E-14	1.18E-14	1.18E-14	1.18E-14	9.21E-15
CGD	7.63E-15	7.63E-15	7.63E-15	7.63E-15	5.11E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	B32	BD19	BD20	BD21	BD22
MODEL	G1	G1	G1	G1	G1
ID	2.87E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	4.68E-03	8.50E-01	8.50E-01	8.50E-01	8.50E-01
VDS	2.41E+00	8.50E-01	8.50E-01	8.50E-01	8.50E-01
GM	4.21E-03	2.68E-03	2.68E-03	2.68E-03	2.68E-03
GDS	1.34E-04	4.71E-03	4.71E-03	4.71E-03	4.71E-03
CGS	9.23E-15	1.18E-14	1.18E-14	1.18E-14	1.18E-14
CGD	5.11E-15	7.63E-15	7.63E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	BD23	BD24	B33	B34	BD28

MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.86E-03	2.86E-03	2.85E-03
VGS	8.50E-01	8.50E-01	0.00E+00	9.14E-04	8.50E-01
VDS	8.50E-01	8.50E-01	2.49E+00	2.41E+00	8.50E-01
GM	2.68E-03	2.68E-03	4.22E-03	4.21E-03	2.68E-03
GDS	4.71E-03	4.71E-03	1.32E-04	1.34E-04	4.71E-03
CGS	1.18E-14	1.18E-14	9.21E-15	9.22E-15	1.18E-14
CGD	7.63E-15	7.63E-15	5.04E-15	5.11E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD29	BD30	BD31	BD32	BD33
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.50E-01	8.50E-01	8.50E-01	8.50E-01	8.50E-01
VDS	8.50E-01	8.50E-01	8.50E-01	8.50E-01	8.50E-01
GM	2.68E-03	2.68E-03	2.68E-03	2.68E-03	2.68E-03
GDS	4.71E-03	4.71E-03	4.71E-03	4.71E-03	4.71E-03
CGS	1.18E-14	1.18E-14	1.18E-14	1.18E-14	1.18E-14
CGD	7.63E-15	7.63E-15	7.63E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B35	B36	B37	B38	B39
MODEL	G1	G1	G1	G1	G1
ID	2.96E-03	2.86E-03	2.87E-03	2.86E-03	2.85E-03
VGS	0.00E+00	-2.64E-03	3.79E-04	0.00E+00	0.00E+00
VDS	2.49E+00	2.52E+00	2.52E+00	2.44E+00	2.41E+00
GM	4.22E-03	4.22E-03	4.22E-03	4.21E-03	4.20E-03
GDS	1.32E-04	1.31E-04	1.32E-04	1.33E-04	1.34E-04
CGS	9.21E-15	9.20E-15	9.21E-15	9.21E-15	9.21E-15
CGD	5.04E-15	5.02E-15	5.02E-15	5.09E-15	5.11E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B40	B41	B42	B43	BD34
MODEL	G1	G1	G1	G1	G1
ID	5.72E-03	2.86E-03	2.87E-03	2.86E-03	2.85E-03
VGS	0.00E+00	-3.86E-03	-1.76E-03	2.17E-03	8.51E-01
VDS	2.48E+00	2.56E+00	2.59E+00	2.41E+00	8.51E-01
GM	8.43E-03	4.22E-03	4.23E-03	4.21E-03	2.68E-03
GDS	2.65E-04	1.31E-04	1.31E-04	1.34E-04	4.71E-03
CGS	1.84E-14	9.19E-15	9.20E-15	9.22E-15	1.18E-14
CGD	1.01E-14	4.98E-15	4.96E-15	5.11E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD35	BD36	BD37	BD38	BD39
MODEL	G1	G1	G1	G1	G1
ID	2.85E-03	2.85E-03	2.85E-03	2.85E-03	2.85E-03
VGS	8.51E-01	8.51E-01	8.51E-01	8.51E-01	8.51E-01
VDS	8.51E-01	8.51E-01	8.51E-01	8.51E-01	8.51E-01
GM	2.68E-03	2.68E-03	2.68E-03	2.68E-03	2.68E-03
GDS	4.71E-03	4.71E-03	4.71E-03	4.71E-03	4.71E-03
CGS	1.18E-14	1.18E-14	1.18E-14	1.18E-14	1.18E-14
CGD	7.63E-15	7.63E-15	7.63E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B44	B45	BD40	BD41	BD42
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.86E-03	2.86E-03	2.86E-03
VGS	0.00E+00	2.37E-03	8.51E-01	8.51E-01	8.51E-01
VDS	2.48E+00	2.41E+00	8.51E-01	8.51E-01	8.51E-01
GM	4.22E-03	4.21E-03	2.68E-03	2.68E-03	2.68E-03

GDS	1.32E-04	1.34E-04	4.71E-03	4.71E-03	4.71E-03
CGS	9.21E-15	9.22E-15	1.19E-14	1.19E-14	1.19E-14
CGD	5.05E-15	5.11E-15	7.63E-15	7.63E-15	7.63E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD43	BD44	BD45	B46	B26
MODEL	G1	G1	G1	G1	G1
ID	2.86E-03	2.86E-03	2.86E-03	2.86E-03	3.13E-03
VGS	8.51E-01	8.51E-01	8.51E-01	0.00E+00	7.50E-02
VDS	8.51E-01	8.51E-01	8.51E-01	2.48E+00	2.51E+00
GM	2.68E-03	2.68E-03	2.68E-03	4.22E-03	4.41E-03
GDS	4.71E-03	4.71E-03	4.71E-03	1.32E-04	1.45E-04
CGS	1.19E-14	1.19E-14	1.19E-14	9.21E-15	9.53E-15
CGD	7.63E-15	7.63E-15	7.63E-15	5.05E-15	5.10E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B27	BD25	BD26	BD27	B28
MODEL	G1	G1	G1	G1	G1
ID	3.13E-03	3.12E-03	3.12E-03	3.12E-03	1.63E-02
VGS	0.00E+00	8.12E-01	8.12E-01	8.12E-01	0.00E+00
VDS	5.05E+00	8.12E-01	8.12E-01	8.12E-01	2.52E+00
GM	4.65E-03	2.97E-03	2.97E-03	2.97E-03	2.41E-02
GDS	1.26E-04	5.51E-03	5.51E-03	5.51E-03	7.51E-04
CGS	9.15E-15	1.33E-14	1.33E-14	1.33E-14	5.25E-14
CGD	3.75E-15	8.72E-15	8.72E-15	8.72E-15	2.86E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B29	B30	B31
MODEL	G1	G1	G1
ID	1.63E-02	1.63E-02	1.63E-02
VGS	2.67E-03	3.94E-04	0.00E+00
VDS	2.44E+00	2.51E+00	2.52E+00
GM	2.40E-02	2.41E-02	2.41E-02
GDS	7.61E-04	7.53E-04	7.51E-04
CGS	5.26E-14	5.25E-14	5.25E-14
CGD	2.90E-14	2.86E-14	2.86E-14
CDS	0.00E+00	0.00E+00	0.00E+00

**** SMALL-SIGNAL CHARACTERISTICS

V(41)/VIN1 = 1.008E+02

INPUT RESISTANCE AT VIN1 = 8.065E+11

OUTPUT RESISTANCE AT V(41) = 5.012E+01

JOB CONCLUDED

TOTAL JOB TIME 64.81

Appendix 2. PSpice simulation for the Larson's Operational Amplifier with compensation

```
******* 03/31/92 ******* PSpice 4.03 - January, 1990 ******* 11:54:43 *******

Larson's GaAs Compensated OP_AMP

****     CIRCUIT DESCRIPTION

*******************************************************************************


Vin  12  0  AC  1m
VDD  20  0  DC  5
VSS  1   0  DC -5
VREF 5   0  DC -3.3
*
* First stage or bootstrapped enhancement stage
B1  10 12  6 G1 0.4
B2  11  0  6 G1 0.4
B3  18 11 10 G1 0.1
B4  17 11 11 G1 0.025
B5  20 17 18 G1 0.4
B6  20 10 17 G1 0.1
B7  6  5  3  G1 0.05
B8  3  1  1  G1 0.05
* Second stage or output stage
B9  20 17 19  G1 0.05
B10 19 11 15  G1 0.05
B11 8  5  2   G1 0.05
B12 2  1  1   G1 0.05
B13 20 15 7   G1 0.117
B14 7  8  16  G1 0.117
B15 16 5  4   G1 0.117
B16 4  1  1   G1 0.117
* Mesfet connected diodes
BD1 15 15 14 G1 0.05
BD2 14 14 13 G1 0.05
BD3 13 13 25 G1 0.05
BD4 25 25 8  G1 0.05
* Compensation Capacitors
Cc1 11 60 0.18pf
Rc1 60 0 0.05k
** ANALYSIS
.MODEL G1 GASFET(level=1 VTO=-1.5  BETA=0.07 LAMBDA=0.05 RD=1 RS=1
+                VBI=0.8 CGS=0.5E-12 CGD=0.5E-12 IS=1E-14 FC=0.5)
*
.TF V(16) Vin
.OP
.AC DEC 10 1K 100G
.PROBE
.END
```

******* 03/31/92 ******* PSpice 4.03 - January, 1990 ******* 11:54:43 *******

Larson's GaAs Compensated OP_AMP

**** GaAs MESFET MODEL PARAMETERS

****

	G1
LEVEL	1
VTO	-1.5
VBI	.8
ALPHA	2
B	.3
BETA	.07
LAMBDA	.05
RD	1
RS	1
CGD	500.000000E-15
CGS	500.000000E-15

******* 03/31/92 ******* PSpice 4.03 - January, 1990 ******* 11:54:43 *******

Larson's GaAs Compensated OP_AMP

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-5.0000	(2)	-3.2391	(3)	-3.2214	(4)	-3.2386
(5)	-3.3000	(6)	1.1552	(7)	2.7493	(8)	.4579
(10)	3.5289	(11)	2.7565	(12)	0.0000	(13)	1.5944
(14)	2.1627	(15)	2.7310	(16)	.4768	(17)	4.2603
(18)	4.8957	(19)	4.1102	(20)	5.0000	(25)	1.0261
(60)	0.0000						

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
Vin	4.692E-12
VDD	-3.009E-02
VSS	3.009E-02
VREF	1.220E-11

TOTAL POWER DISSIPATION 3.01E-01 WATTS

******* 03/31/92 ******* PSpice 4.03 - January, 1990 ******* 11:54:43 ***

Larson's GaAs Compensated OP_AMP

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** GASFETS

NAME	B1	B2	B3	B4	B5
MODEL	G1	G1	G1	G1	G1
ID	3.53E-03	3.41E-03	3.53E-03	3.41E-03	3.53E-03
VGS	-1.16E+00	-1.16E+00	-7.72E-01	0.00E+00	-6.35E-01
VDS	2.37E+00	1.60E+00	1.37E+00	1.50E+00	1.04E-01
GM	2.10E-02	2.03E-02	1.02E-02	4.99E-03	8.26E-03
GDS	1.60E-04	2.06E-04	3.24E-04	3.58E-04	4.02E-02
CGS	1.28E-13	1.28E-13	3.53E-14	1.16E-14	1.49E-13
CGD	8.61E-14	9.50E-14	2.62E-14	7.59E-15	1.45E-13
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B6	B7	B8	B9	B10
MODEL	G1	G1	G1	G1	G1
ID	3.41E-03	6.94E-03	6.94E-03	6.93E-03	6.93E-03
VGS	-7.31E-01	-7.86E-02	0.00E+00	1.50E-01	2.54E-02
VDS	7.40E-01	4.38E+00	1.78E+00	8.90E-01	1.38E+00
GM	9.27E-03	1.08E-02	1.02E-02	9.17E-03	1.00E-02
GDS	2.03E-03	2.88E-04	4.60E-04	5.16E-03	1.00E-03
CGS	3.57E-14	2.22E-14	2.31E-14	2.52E-14	2.34E-14
CGD	2.99E-14	9.89E-15	1.43E-14	1.89E-14	1.58E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B11	B12	B13	B14	B15
MODEL	G1	G1	G1	G1	G1
ID	6.93E-03	6.93E-03	1.62E-02	1.62E-02	1.62E-02
VGS	-6.09E-02	0.00E+00	-1.83E-02	-1.90E-02	-6.14E-02
VDS	3.70E+00	1.76E+00	2.25E+00	2.27E+00	3.72E+00
GM	1.07E-02	1.02E-02	2.42E-02	2.42E-02	2.50E-02
GDS	2.96E-04	4.69E-04	7.87E-04	7.82E-04	6.92E-04
CGS	2.24E-14	2.31E-14	5.35E-14	5.35E-14	5.23E-14
CGD	1.06E-14	1.44E-14	3.06E-14	3.05E-14	2.48E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B16	BD1	BD2	BD3	BD4
MODEL	G1	G1	G1	G1	G1
ID	1.62E-02	6.93E-03	6.93E-03	6.93E-03	6.93E-03
VGS	0.00E+00	5.68E-01	5.68E-01	5.68E-01	5.68E-01
VDS	1.76E+00	5.68E-01	5.68E-01	5.68E-01	5.68E-01
GM	2.38E-02	7.18E-03	7.18E-03	7.18E-03	7.18E-03
GDS	1.10E-03	1.95E-02	1.95E-02	1.95E-02	1.95E-02

CGS	5.40E-14	3.67E-14	3.67E-14	3.67E-14	3.67E-14
CGD	3.36E-14	2.75E-14	2.75E-14	2.75E-14	2.75E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

**** SMALL-SIGNAL CHARACTERISTICS

V(16)/Vin = 1.087E+02

INPUT RESISTANCE AT Vin = -9.076E+09

OUTPUT RESISTANCE AT V(16) = 5.037E+01

JOB CONCLUDED

TOTAL JOB TIME 13.84

Appendix 3. PSpice simulation for the Toumazou's Operational Amplifier with compensation

```
Toumazou's GaAs Compensated OP_AMP

****      CIRCUIT DESCRIPTION

*******************************************************************************


VSS1 11 0  DC -5
VSS2 20 0  DC -7
Vin 15  0  AC 1m
VDD 30  0  DC  5
** Differential to single ended converter
B1 17 15 16 G1 0.3
B2 30 0  16 G1 0.3
B3 30 19 17 G1 0.015
B4 16 9  11 G1 0.01
B5 16 11 11 G1 0.02
B6 9  20 20 G1 0.02
B7 30 17 19 G1 0.02
** Level shifter
BD1 19 19 21 G1 0.01
BD2 21 21 22 G1 0.01
BD3 22 22 23 G1 0.01
BD4 23 23 24 G1 0.01
BD5 24 24 25 G1 0.01
BD6 25 25 26 G1 0.01
BD7 26 26 27 G1 0.017
BD8 27 27  9 G1 0.025
** Double cascode current mirror
B8  30 4  5  G1 0.1
B9  5  4  6  G1 0.01
B10 6  11 10 G1 0.1
B11 10 9  11 G1 0.01
B12 7  9  11 G1 0.02
B13 4  10  7 G1 0.06
B14 2  6  4  G1 0.02
B15 30 5  2  G1 0.06
** Class A output stage
B16 30 50 40 G1 0.1
B17 40 11 11 G1 0.1
* Frequency compensation : pole zero cancellation
C1 50  0  4P
R1  4  50 10
** ANALYSIS
.MODEL G1 GASFET(level=1 VTO=-1.5  BETA=0.07 LAMBDA=0.05 RD=1 RS=1
+                VBI=0.8 CGS=0.5E-12 CGD=0.5E-12 IS=1E-14 FC=0.5)
.TF V(40) Vin
.OP
.AC DEC 10 1K 100G
.PROBE
.END
```

Toumazou's GaAs Compensated OP_AMP

**** GaAs MESFET MODEL PARAMETERS

****

	G1
LEVEL	1
VTO	-1.5
VBI	.8
ALPHA	2
B	.3
BETA	.07
LAMBDA	.05
RD	1
RS	1
CGD	500.000000E-15
CGS	500.000000E-15

Toumazou's GaAs Compensated OP_AMP

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(2)	1.9058	(4)	.1154	(5)	1.2103	(6)	.1153
(7)	-3.2041	(9)	-5.0003	(10)	-3.9033	(11)	-5.0000
(15)	0.0000	(16)	1.1677	(17)	2.1762	(19)	2.2018
(20)	-7.0000	(21)	1.1904	(22)	.1791	(23)	-.8323
(24)	-1.8436	(25)	-2.8550	(26)	-3.8664	(27)	-4.5286
(30)	5.0000	(40)	.1094	(50)	.1154		

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VSS1	2.458E-02
VSS2	2.805E-03
Vin	3.350E-12
VDD	-2.738E-02

TOTAL POWER DISSIPATION 2.79E-01 WATTS

Toumazou's GaAs Compensated OP_AMP

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** GASFETS

NAME	B1	B2	B3	B4	B5
MODEL	G1	G1	G1	G1	G1
ID	2.24E-03	2.62E-03	2.24E-03	1.62E-03	3.24E-03
VGS	-1.17E+00	-1.17E+00	2.56E-02	-3.25E-04	0.00E+00
VDS	1.01E+00	3.83E+00	2.82E+00	6.17E+00	6.17E+00
GM	1.38E-02	1.62E-02	3.25E-03	2.42E-03	4.84E-03
GDS	4.44E-04	1.10E-04	1.00E-04	6.26E-05	1.25E-04
CGS	9.55E-14	9.54E-14	6.98E-15	4.56E-15	9.12E-15
CGD	7.79E-14	5.58E-14	3.61E-15	1.71E-15	3.43E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B6	B7	BD1	BD2	BD3
MODEL	G1	G1	G1	G1	G1
ID	2.81E-03	2.81E-03	2.62E-03	2.62E-03	2.62E-03
VGS	0.00E+00	-2.56E-02	1.01E+00	1.01E+00	1.01E+00
VDS	2.00E+00	2.80E+00	1.01E+00	1.01E+00	1.01E+00
GM	4.13E-03	4.21E-03	2.35E-03	2.35E-03	2.35E-03
GDS	1.52E-04	1.26E-04	3.41E-03	3.41E-03	3.41E-03
CGS	9.22E-15	9.10E-15	1.00E-14	1.00E-14	1.00E-14
CGD	5.48E-15	4.79E-15	6.10E-15	6.10E-15	6.10E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	BD4	BD5	BD6	BD7	BD8
MODEL	G1	G1	G1	G1	G1
ID	2.62E-03	2.62E-03	2.62E-03	2.81E-03	2.81E-03
VGS	1.01E+00	1.01E+00	1.01E+00	6.62E-01	4.72E-01
VDS	1.01E+00	1.01E+00	1.01E+00	6.62E-01	4.72E-01
GM	2.35E-03	2.35E-03	2.35E-03	2.81E-03	3.02E-03
GDS	3.41E-03	3.41E-03	3.41E-03	6.53E-03	9.82E-03
CGS	1.00E-14	1.00E-14	1.00E-14	1.35E-14	1.68E-14
CGD	6.10E-15	6.10E-15	6.10E-15	9.54E-15	1.35E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

NAME	B8	B9	B10	B11	B12
MODEL	G1	G1	G1	G1	G1
ID	1.28E-03	1.28E-03	1.28E-03	1.28E-03	2.78E-03
VGS	-1.09E+00	7.81E-05	-1.10E+00	-3.25E-04	-3.25E-04
VDS	3.79E+00	1.09E+00	4.02E+00	1.10E+00	1.80E+00
GM	6.53E-03	1.87E-03	6.56E-03	1.87E-03	4.08E-03
GDS	5.39E-05	4.19E-04	5.34E-05	4.17E-04	1.80E-04

CGS	3.24E-14	4.64E-15	3.24E-14	4.64E-15	9.23E-15
CGD	1.88E-14	3.36E-15	1.84E-14	3.36E-15	5.71E-15
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NAME	B13	B14	B15	B16	B17
MODEL	G1	G1	G1	G1	G1
ID	2.78E-03	2.78E-03	2.78E-03	1.57E-02	1.57E-02
VGS	-6.99E-01	-7.81E-05	-6.96E-01	5.97E-03	0.00E+00
VDS	3.32E+00	1.79E+00	3.09E+00	4.89E+00	5.11E+00
GM	7.36E-03	4.08E-03	7.32E-03	2.32E-02	2.33E-02
GDS	1.20E-04	1.81E-04	1.21E-04	6.37E-04	6.32E-04
CGS	2.16E-14	9.23E-15	2.16E-14	4.59E-14	4.57E-14
CGD	1.23E-14	5.71E-15	1.26E-14	1.90E-14	1.86E-14
CDS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

**** SMALL-SIGNAL CHARACTERISTICS

V(40)/Vin = 1.609E+03

INPUT RESISTANCE AT Vin = 1.367E+11

OUTPUT RESISTANCE AT V(40) = 5.085E+01

JOB CONCLUDED

TOTAL JOB TIME 23.67